Low Frequency Ring Oscillator and Its Use in Non Overlapping Clock Generation

Rishi Todani, Ashis Kumar Mal, and Kanchan Baran Maji

***Abstract*—Switched capacitor (SC) techniques have become the default standard for implementing mixed signal blocks in CMOS technologies. Non-overlapping clock (NOC) generator is a key building block for SC circuits, traditionally implemented using inverter chains. For moderate and high frequencies, the numbers of inverter stages are nominal. But for low frequency applications, like biomedical signal processing, the numbers of inverters increase significantly affecting the area and power budget of the design. In this work, three new inverter cells are proposed for realizing low frequency ring oscillator. They exhibit a delay larger than other popular implementation techniques. Simulation results show that low frequency oscillations can be achieved with much lesser number of transistors and with lower power dissipation. The proposed inverter is then used to realize a voltage controlled NOC generator whose non-overlap period can be modulated. Alternate digital multiplexing technique is also presented to control the non-overlap period.**

***Index Terms*—Ring oscillator, NOC generator, switched capacitor circuits, inverter.**

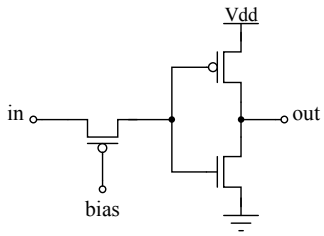

Fig. 1. Proposed inverter.

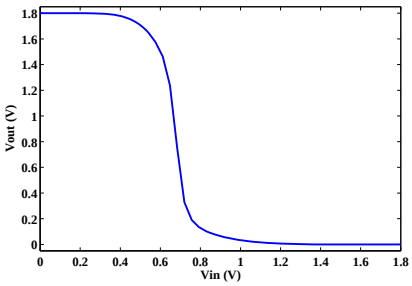

Fig. 2. VTC of proposed inverter

I. Introduction

Switched capacitor techniques have gained popularity in analog and mixed signal design. This is primarily due to the fact that SC circuits exhibit high accuracy and low temperature invariance along with other advantages [1], [2]. Analog blocks like SC integrators, filters and comparators [3] and mixed signal blocks like analog to digital converters (ADC), sigma delta modulators and sampled analog architectures [4], [5] employ SC circuits extensively. Non-overlapping clock generator is one of the key building blocks of an SC circuit. Numerous techniques for clock generation are proposed in [6]–[9].

An inverter circuit exists in literature, which uses transmission gate (TG) before the static CMOS inverter to increase and control the delay by applying a suitable bias. However, due to parallel connection of NMOS and PMOS in a TG, the delay does not increase significantly. It should be noted that if one of the transistors in TG is removed, a larger delay could be achieved. Thus, NMOS becomes the obvious choice as the transistor to be removed from this circuit. Since PMOS will exhibit a larger delay than a TG, the overall delay of the inverter cell increases. Even though the PMOS pass gate reduces the signal swing by $|V_{Tp}|$, the static CMOS inverter can easily restore this signal swing to almost rail to rail.

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II. Signal Swing of Proposed Inverter Cell

The proposed inverter cell is as shown in Fig. 1 and its voltage transfer characteristic (VTC) is shown in Fig. 2. The gate terminal of the PMOS pass gate is connected to 0 V. Using the principles of pass gate, when the input to the circuit is logic 1, i.e. V_{DD}, the PMOS pass gate passes this signal without any degradation. Thus, the input to the CMOS inverter is at strong logic 1, i.e. V_{DD}. On the other hand, when the input to the circuit is logic 0, i.e. 0 V, the input to the static CMOS inverter becomes weak logic 0, i.e. $|V_{Tp}|$, since PMOS passes bad 0. Even with this degraded input, the static CMOS inverter restores the signal level to V_{DD}. This is primarily due to the fact that, the static CMOS inverter offers a good gain ($-dVO/dt > 1$) between V_{IL} and V_{IH}. Roughly speaking, this is behavior starts when NMOS is turned ON, and lasts up to when PMOS is turned OFF. This represents the entire input range except from 0 to V_{Tn} and $V_{DD} - |V_{Tp}|$ to V_{DD}. The regions where the voltage transfer characteristics (VTC) are flat, the inverter offers no gain. As a result, the inverter is capable of restoring the signal level from $|V_{Tp}|$ to V_{DD} to almost rail-to-rail. Thus, even though the input to the CMOS inverter is $|V_{Tp}|$ to V_{DD}, the output swings from rail to rail.

III. Delay Calculation

In this section, we analytically analyze the delay of the proposed inverter cell. The overall delay of the proposed inverter cell is the sum of the delays offered by the PMOS pass gate and the CMOS inverter.

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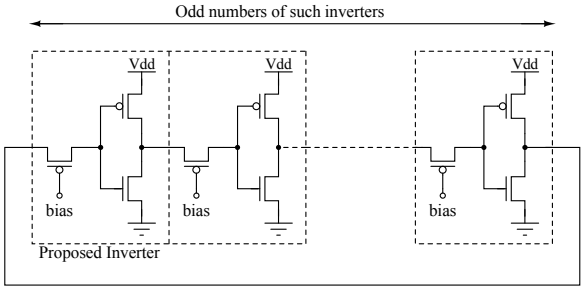

Fig. 3. Ring oscillator using proposed inverter.

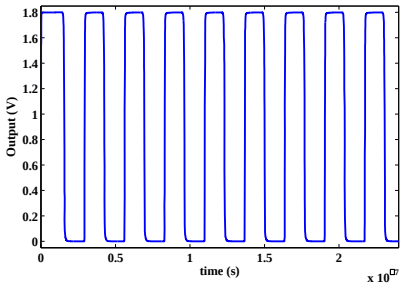

Fig. 4. Ring oscillator output.

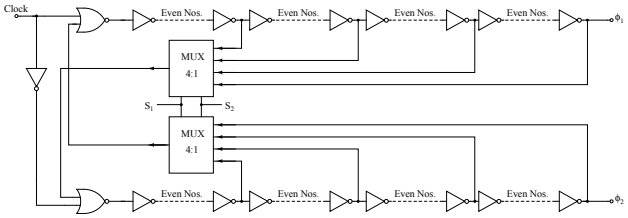

Fig. 5. Digitally controllable NOC generator.

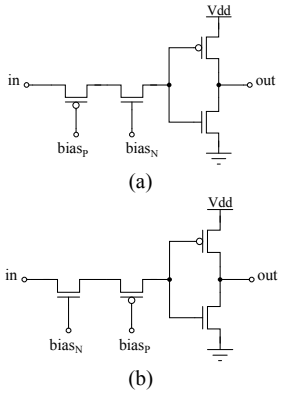

Fig. 6. Alternate inverter implementation.

TABLE I: PROPOSED INVERTER DELAY.

	Delay reported by Spectre
τ_{pLH}	1.73 ns
τ_{pHL}	119.4 ps

TABLE II: NOC GENERATION.

Gate Potential of PMOS Pass Gate	Non Overlap Period
0 V	17.3 ns
0.05 V	37.3 ns
0.10 V	94.1 ns
0.15 V	270.4 ns
0.20 V	926.9 ns
0.25 V	3.39 µs
0.30 V	13.31 µs
0.35 V	54.72 µs
0.40 V	235 µs

TABLE III: DELAY COMPARISON OF INVERTER CELLS.

	Inverter Cell in Fig.1	Inverter Cell in Fig.6(a)	Inverter Cell in Fig.6(b)
τ_{pLH}	1.73 ns	2.55 ns	1.76 ns
τ_{pHL}	119.40 ps	169.44 ps	154.11 ps

A. Pass Gate Delay

By the pass gate principles, the delay introduced by the PMOS pass gate is given by,

$$\tau_p(pmos) = 0.7 R_p \frac{C_{ox}}{2} \tag{1}$$

where, R_p is an estimate for the resistance between the drain and source of the PMOS and is given by:

$$R_p = \frac{2V_{DD}L}{K_p W (V_{DD} - |V_{Tp}|)^2} \tag{2}$$

B. CMOS Inverter Delay

For simplicity, it is assumed at $V_{Tn} = |V_{Tp}|$. As already mentioned, the input to the CMOS inverter swings from $|V_{Tp}|$ to V_{DD}. Thus, when input switches from $|V_{Tp}|$ to V_{DD}, the output switches from V_{DD} to 0 V. Therefore, the high-to-low delay expression holds true for the proposed circuit. However, when input to the CMOS inverter is weak logic 0, i.e. $|V_{Tp}|$, the output switches from 0 to V_{DD} where PMOS charges the load with saturated current. Various inverter delay estimation techniques are given in [10]–[15]. As per the signal transition, the low-to-high delay expression is modified as:

$$\tau_{pHL}(inv) = C_{load} \int_{V_{out}=0}^{V_{out}=2V_{Tp}} \frac{dV_{out}}{i_{Dp}(sat)} \tag{3}$$

Solving the above expression gives,

$$\tau_{pHL}(inv) = \frac{2C_{load}\,|V_{Tp}|}{K_p(V_{DD} - 2|V_{Tp}|)} \tag{4}$$

High to low delay of the inverter is given by,

$$\tau_{pHL}(inv) = \frac{C_{load}/K_n}{V_{DD} - V_{Tn}} \times \left[\frac{2V_{Tn}}{V_{DD} - V_{Tn}} + \ln\left[\frac{4(V_{DD} - V_{Tn})}{V_{DD}} - 1 \right] \right] \tag{5}$$

C. Proposed Inverter Delay

The delay of the proposed inverter cell is the sum of the delay offered by the pass gate and that of the degraded input CMOS inverter. Thus, the low-to-high and high-to-low delay of the proposed inverter cell is given by:

$$\tau_{pLH}(tot) = \tau_p(pmos) + \tau_{pLH}(inv) \quad (6)$$

$$\tau_{pHL}(tot) = \tau_p(pmos) + \tau_{pHL}(inv) \quad (7)$$

It should be noted that apart from the fact that PMOS pass gate increases the delay of the inverter, the delay of the CMOS inverter itself increases due to the degraded signal swing. For simplicity, we have considered that $|V_{Tp}| = V_{Tn}$. However, practically $|V_{Tp}| > V_{Tn}$. This means that when input to the CMOS inverter is at weak logic 0, i.e. $|V_{Tp}|$, the NMOS transistor is also conducting. Thus, PMOS tries to charge the load and NMOS tries to discharge simultaneously. Thus, signal contention will occur which increases the delay further. To incorporate this phenomenon in the presented analytical model, the expression for low-to-high (LH) delay of the inverter needs to be modified and discharging of load through NMOS should be included.

IV. Simulation

The proposed inverter cell was implemented using proprietary 180 nm CMOS Process. Cadence Spectre with BSIM3v3 model was used to obtain the delay values and the results are shown in Table I.

A. Ring Oscillator

Several ring oscillator structures have been simulated starting from seven stages. The oscillations obtained using a ring with eleven number of proposed inverter cells is shown in Fig. 4, with bias voltage at 0.

B. Controlled NOC Generator

Standard method for NOC generation uses delay blocks, two NAND/NOR gates and an inverter to derive two phase non-overlapping clocks from a reference clock. Even number of proposed inverter cells may be used to implement the delay blocks. The non-overlap period of the generated two phase clock is directly proportional to the delay of the delay block. As mentioned earlier, the delay of the proposed inverter can be controlled by modulating the gate potential of the PMOS pass gate. With the increase in the gate potential, the delay of the proposed inverter cell increases. This in turn will increase the non-overlap period of the two phase non-overlapping clock. Table II depicts the increase in non-overlap period with the increase in PMOS gate potential.

Digital multiplexing technique may also be employed to modulate the non-overlap period of the NOC generator. A simple scheme to achieve this is shown in Fig. 5. The multiplexer chooses which feedback path connects to the input of the NOR gates. Thus, the total numbers of inverter cells in the delay chain can me controlled and this directly controls the non-overlap period. Two select lines, S1 and S2, may be used to select the appropriate feedback path.

V. Alternate Implementation

There are two more alternatives to the proposed inverter. An NMOS pass gate may be squeezed between the PMOS pass gate and the inverter, as shown in Fig. 6(a), or an NMOS pass gate preceding the PMOS pass gate as shown in Fig. 6(b). The delay associated with NMOS pass gate is given by:

$$\tau_n(nmos) = 0.7R_n \frac{C_{ox}}{2} \quad (8)$$

where *Rn* is an estimate for the resistance between the drain and source of the NMOS and is given by:

$$R_n = \frac{2V_{DD}L}{K_n W(V_{DD} - V_{Tn})^2} \quad (9)$$

If the circuits given in Fig. 6 are used, then (8) must be added to (7) and (6). Also, it should be noted that since the input to the inverter will now swing between $|V_{Tp}|$ and $V_{DD} - V_{Tn}$, the expression for the propagation delay of the inverter has to be modified accordingly. It is interesting to note that addition of NMOS will slow down the operation due to two reasons. Firstly, simply because of the increase in the input resistance and capacitance of the proposed inverter cell; secondly, due to further degradation of input signal swing of the inverter this leads to lower overdrive for charging of discharging the load. Circuits given in Fig. 6 may also be used in controllable NOC generation with appropriate gate biases. It is to be mentioned that complementary bias voltages may be needed if the circuits given in Fig. 6 are to be voltage controlled. If we consider that the gate of PMOS ($bias_P$) is at V_X, then gate of NMOS ($bias_N$) may be kept at $V_{DD} - V_X$. Alternately, $bias_N$ may be kept at some fixed potential and only $bias_P$ be varied. Using these schemes, a wide controllable range of non-overlapping period may be achieved.

VI. Conclusion

This paper presents a simple scheme for generating more delay using lesser number of transistors. It is shown that if a CMOS inverter is preceded with a PMOS pass gate, a larger delay can be realized without any compromise on the signal swing. Also, the gate potential of the pass gate can be modulated to achieve variable delay. The analytical expression for the delay of the proposed inverter cell is derived. The circuit when simulated as a ring oscillator is found to have significant delay and thus lesser number of transistors would be required to obtain a desired frequency. An NOC generator is then designed whose non-overlap period can be modulated by controlling the gate bias of the PMOS pass gate. Alternate inverter cells realization is also presented and their delay values are reported. Finally, an NOC generator with digital multiplexing scheme is presented whose non-overlap period can be controlled digitally.

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