A 6-bit 2GS/s Low Power Flash ADC

Jyun-Syong Lai and Zhi-Ming Lin

***Abstract*—In this paper a 6-bit Flash Analog-to-Digital converter (ADC) implemented in TSMC 0.18-µm CMOS process is presented. Different from the conventional Flash ADCs, the architecture of the proposed ADC is based on single-ended comparators with a sample-and-hold (S/H) circuit. Single-ended comparators are formed using only inverters and resistors. Therefore, our design can reduce a lot of transistor numbers and power consumption. The designed ADC consumes 0.425 mW at 1.5V power supply. The speed of this design is 2 GS/s. The simulated static differential non-linearity error (DNL) and integral non-linearity error (INL) are between 0.4/-0.29 LSB and 0.4/-0.39 LSB, respectively.**

***Index Terms*—Analog-to-digital converter, comparator, flash, inverter.**

I. Introduction

In recent years, the wireless portable applications become more and more popular. High-speed low-resolution ADCs are an essential part of receivers for wireless standards. Speed and power consumption are the key parameters for the wireless portable applications. For high-speed applications, flash ADC is often used for its fast speed compared with the other known ADC architectures. However, the transistor number and power consumption of this architecture depends exponentially on the bit number of resolution. It requires 2^n - 1 comparators for an n-bit ADC. Since chip cost is usually proportional to the chip size, large chip size will bring in unacceptable cost.

The pipelined architecture [1] and the successive approximation (SAR) [2] architecture have been proposed to improve the transistor number and power consumption of the flash ADC. But, they can only achieve medium speed (MS/s). They cannot meet the high speed of applications.

The time interleaving (TI) architecture is often used to increase the speed of medium speed ADC. A TI ADC comprises several analog-to-digital (A/D) channels, and coordinates their operation so that the analog input is sampled and converted sequentially by different A/D channels. Different types of A/D channels have been used, including pipelined ADCs [3][4][5] and SAR ADCs [6]. But, this kind of architecture still exist some shortcomings. The series one is that power consumption will increase accordingly with the increase of channels of the TI ADC.

In this paper, we present a 6-bit Flash ADC in TSMC 0.18-µm process. By the design of single-ended comparators with S/H circuit, the proposed ADC accomplishes high sample speed and low power consumption. The sample speed is 2GS/s. The power consumption is only 0.425mW at 1.5V power supply. The simulated static differential non-linearity error (DNL) and integral non-linearity error (INL) are between 0.4/-0.29 LSB and 0.4/-0.39 LSB, respectively. After introduction, Section Ⅱ will discuss the architecture of the proposed Flash ADC. Section Ⅲ will present simulation results. Section Ⅳ will make some conclusions.

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Jyun-Syong Lai is with the Graduate Program of Integrated Circuit Design of Computer Science and Information Engineering, National Changhua University of Education.

Zhi-Ming Lin is with the Department of Computer Science and Information Engineering, National Changhua University of Education (e-mail: zmlin@cc.ncue.edu.tw)

II. Circuit Design

Fig. 1 shows the block diagram of the presented 6-bit flash ADC. This ADC is composed of resistors, S/H circuits, comparators, buffers, and a thermometer code to binary code encoder.

The S/H circuit samples the voltage of a continuously varying analog input and holds voltage value. The reference voltage is subdivided in a set of resistors These voltages are compared with the output of S/H circuit by comparators. The output of comparator is a kind of thermometer code. The encoder converts the thermometer code to set of binary codes $B_{0\sim5}$.

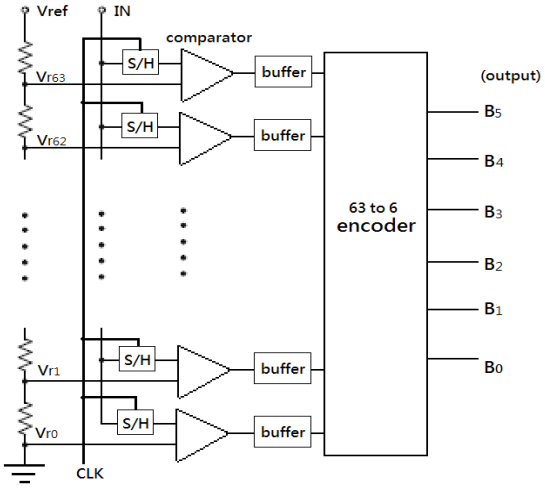

Fig. 1. The presented 6-bit flash ADC.

A. Sample-and-Hold Circuit

The S/H circuit is used in ADC to eliminate variations in input signal that can corrupt the conversion process. In the comparison process, the delay time of comparator is less than the delay time of encoder. If the input of comparator was changed during the comparison process, the resulting conversion would be inaccurate and possibly completely unrelated to the true input value. The S/H circuit of the proposed ADC is shown in Fig. 2. When the CLK=1, the S1 is open and the S/H circuit samples the voltage of IN. When the CLK=0, the S1 is close and the S/H circuit holds the voltage sampled at CLK=1. In order to address the signal-dependent charge injection from S1 onto Vi, S2 was added and sized to have one-half the W/L of S1.

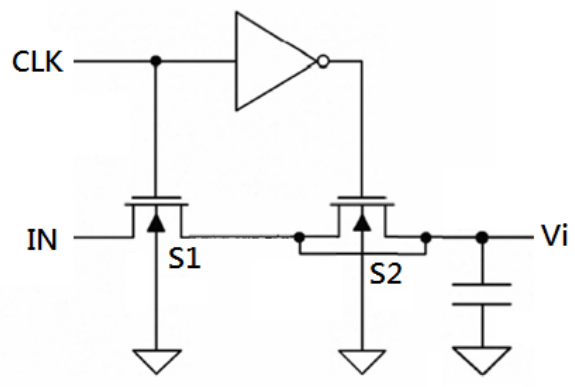

Fig. 2. The architecture of S/H circuit.

B. Single-Ended Comparator

In the traditional flash ADC, comparators need lots of transistor number and power consumption. We design a single-ended comparator to improve the traditional flash ADC. The single-ended comparator consists of a CMOS inverter as shown in Fig. 3. The threshold voltage (V_{th}) of NMOS can be expressed as (1)

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right) \quad (1)$$

Vth0 is threshold voltage when source and bulk is connected together, γ is body effect parameter and Φf is semiconductor parameter. V_{SB} is set to 0 to avoid the body effect. The MOS operating mechanism is depended on the relationship of V_{GS} and Vth.

By assigning different resistors between the sources of two NMOS transistors, we can change the source voltages of the NMOS transistors. If $V_{GS} < Vth$, NMOS is at the "cut-off" region, and the comparator will output a negative logic "0". If $V_{GS} > Vth$, NMOS is at the "saturation" region, and the comparator will output a negative logic "1".

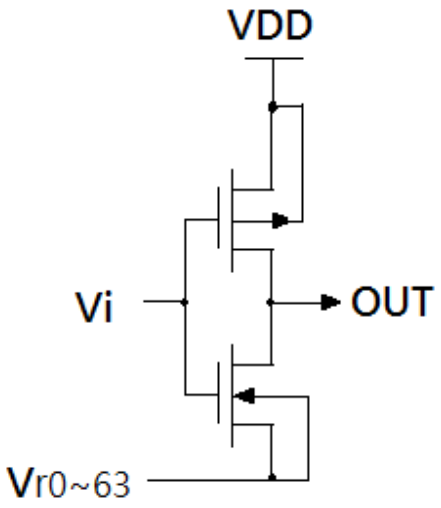

Fig. 3. The presented single-ended comparator.

C. Thermometer Code to Binary Code Encoder

In general, a ADC needs a digital encoding network that converts 2^N-1 thermometer code (TC) inputs to N bit binary code (BC). The usual implementation of encoder has been read-only memory (ROM), programmable logic array (PLA) circuits, XOR encoder and Wallace tree encoder. In this paper, it is implemented by a high speed ROM encoder [7]. The main advantage of this encoder is that the thermometer code is converted to binary code without any intermediate conversion, which is usually implemented using XOR gates or '01' generator circuits. Hence this encoder reduces the number of transistors and increases the speed of ADC. For a six bit ADC, the equations for output binary bits are as shown in (2).

$$\begin{aligned}
B5 &= C31 \\
B4 &= C47 + \overline{C31} \times C15 \\
B3 &= C55 + \overline{C47} \times C39 + \overline{C31} \times C23 + \overline{C15} \times C07 \\
B2 &= C59 + \overline{C55} \times C51 + \overline{C47} \times C43 + \overline{C39} \times C35 + \overline{C31} \times C27 + \overline{C23} \times C19 + \overline{C15} \times C11 + \overline{C07} \times C03 \\
B1 &= C61 + \overline{C59} \times C57 + \overline{C55} \times C53 + \overline{C51} \times C49 + \overline{C47} \times C45 + \overline{C43} \times C41 + \overline{C39} \times C37 + \overline{C35} \times C33 \\
&\quad + \overline{C31} \times C29 + \overline{C27} \times C25 + \overline{C23} \times C21 + \overline{C19} \times C17 + \overline{C15} \times C13 + \overline{C11} \times C09 + \overline{C07} \times C05 + \overline{C03} \times C01 \\
B0 &= C62 + \overline{C61} \times C60 + \overline{C59} \times C58 + \overline{C57} \times C56 + \overline{C55} \times C54 + \overline{C53} \times C52 + \overline{C51} \times C50 + \overline{C49} \times C48 \\
&\quad + \overline{C47} \times C46 + \overline{C45} \times C44 + \overline{C43} \times C42 + \overline{C41} \times C40 + \overline{C39} \times C38 + \overline{C37} \times C36 + \overline{C35} \times C34 + \overline{C33} \times C32 \\
&\quad + \overline{C31} \times C30 + \overline{C29} \times C28 + \overline{C27} \times C26 + \overline{C25} \times C24 + \overline{C23} \times C22 + \overline{C21} \times C20 + \overline{C19} \times C18 + \overline{C17} \times C16 \\
&\quad + \overline{C15} \times C14 + \overline{C13} \times C12 + \overline{C11} \times C10 + \overline{C09} \times C08 + \overline{C07} \times C06 + \overline{C05} \times C04 + \overline{C03} \times C02 + \overline{C01} \times C00
\end{aligned} \quad (2)$$

III. Simulation Results

The performance of the proposed 6-bits Flash ADC was simulated using the HSPICE. The circuit is designed in TSMC 0.18μm CMOS process. The ADC binary outputs are illustrated in Fig. 5. The top waveform of Fig. 5 is the output of the most significant bit (MSB). The bottom waveform of Fig. 5 is the output of the least significant bit (LSB). The row-coordinate of Fig. 5 is time. The simulated DNL of the proposed ADC are illustrated in Fig. 6. The simulated INL of the proposed ADC are illustrated in Fig. 7. Because DNL and INL are <0.5 LSB, this ADC has superior linearity. Table I shows the performance comparison between this ADC and the other reported ADCs. This ADC gets the excellent sample speed and the best results on power consumption.

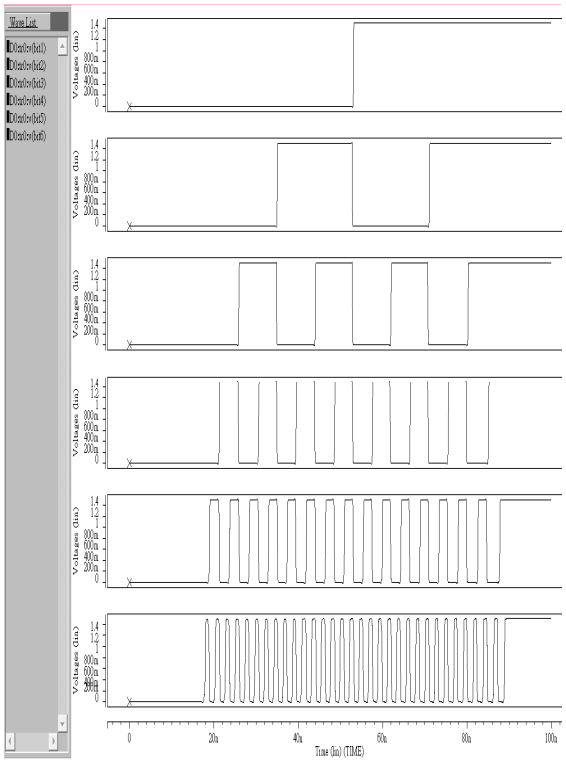

Fig. 4. The ADC binary outputs.

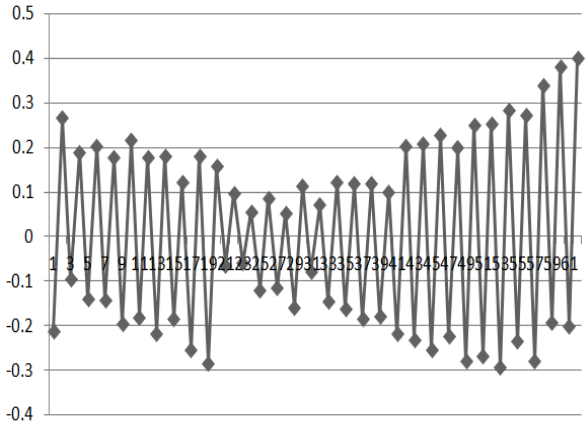

Fig. 5. Simulated DNL of the proposed ADC.

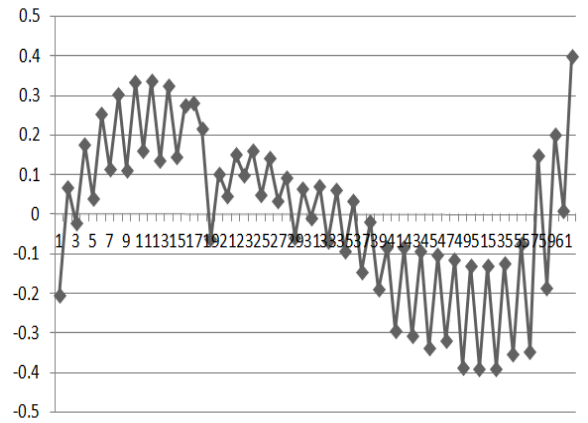

Fig. 6. Simulated INL of the proposed ADC.

TABLE I: PERFORMANCE COMPARISON WITH THE OTHER ADCS.

	[3]	[4]	[5]	[6]	[8]	**This Work**
Resolution (bit)	6	6	6	6	6	**6**
Process (nm)	65	40	130	130	130	**180**
Supply Voltage (V)	1.2	1.1	1.2	1.2	1.2	**1.5**
Sample Speed (GHz)	0.8	2.2	1	1.25	2	**2**
Power (mW)	30	2.6	20	32	170	**0.425**
ADC Architecture	TI-pipeline	TI-pipeline	TI-pipeline	TI-SAR	flash	**flash**

IV. CONCLUSION

A 6-bit Flash Analog-to-Digital converter was designed in TSMC 0.18-µm CMOS process. Due to the single-ended comparators with a sample-and-hold circuit, the proposed ADC not only remains high speed but also reduces a lot of transistor number and power consumption. The supply voltage is 1.5V, and the simulated power consumption is only 0.425mW. Speed of the proposed Analog-to-Digital converter is 2 GS/s. The simulated static differential non-linearity error (DNL) and integral non-linearity error (INL) are between 0.4/-0.29 LSB and 0.4/-0.39 LSB, respectively.

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