Analysis of Gate Leakage Current in IP3 SRAM Bit-Cell under Temperature Variations in DSM Technology

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***Abstract*— In this paper, we present the temperature based simulation and analysis of gate leakage current for the proposed low-stress IP3 SRAM bit cell. In CMOS technologies, cache memory occupies a large die area and this may experience different temperatures. Under temperature variations, performance of the system may degrade. Therefore, in the IP3 SRAM cell, gate leakage has been analyzed under temperature variations. It is observed that with rise in temperature, leakage and standby power dissipation increases. The observation of the effect of temperature variations on standby power indicates that increase in standby power is minimum for P3 cell and IP3 cell, with respect to 6T and PP SRAM cells. The gate leakage observed is minimum in IP3 cell with temperature variations. This work is being carried out at deep-sub micron CMOS technology, 45nm, with t_{ox}=2.4nm, V_{thn}=0.22V, V_{thp}=0.224V, V_{DD}=0.7V and temperature is varied from -25^{0}C to +125^{0}C.**

***Index Terms*—Gate Leakage, IP3-SRAM cell, sub-threshold leakage, SRAM, standby power.**

I. Introduction

At Nano-Scale CMOS technology, power has become a design constraint not only in handheld and mobile devices but also in high performance processors. Dynamic power dissipation occurs due to switching activity in CMOS circuits and static power dissipation occurs due to leakage currents. Therefore, leakage currents are gaining more importance. But with scaling down of CMOS transistors, gate leakage and sub-threshold leakage current increases. The gate leakage is predicted to increase at a rate of 500x per technology generation whereas subthreshold leakage is predicted to increase by 5x [2]. There are several leakage reduction techniques introduced by the researcher community but each has to be checked and verified according to the circuit techniques and target technology without sacrificing the data stability, delay etc.

Temperature dependence of leakage currents is very important in very large scale integration (VLSI) circuits because they operate at elevated temperatures due to power dissipation. Subthreshold leakage consists of major part of leakage. It is expected to increase with rise in temperature. So, reliability becomes a serious concern. As the temperature changes, it affects the leakage and performance of a SRAM bit cell. That's why, thermal analysis of IP3 SRAM bit cell is carried out in this paper. We establish a relationship for gate leakage versus temperature and subthreshold leakage versus temperature.

In this paper, gate leakage current analysis of IP3 SRAM cell is presented on the basis of simulation results. Here, parametric analysis of IP3-SRAM cell is done and temperature is chosen as the parameter. Then, parametric analysis is carried out with temperature range from -250C to +1250C. The simulation results are compared with 6T, PP and P3 SRAM cells. All the simulations are being carried out using 45nm CMOS technology.

The paper is organized as follows: In section II, operation of conventional 6T SRAM bit-cell and basic leakage current mechanisms are given. The section III reviews the IP3, PP and the P3 SRAM cell designs. The section IV presents design and analysis of IP3 cell followed by the analysis of the gate leakage and standby power in 6T, PP, P3 and IP3 cells in section V and conclusion in section VI, respectively.

II. Conventional 6T SRAM Cell

The conventional SRAM cell has six MOS transistors, as shown in Fig.1. Unlike DRAM, it doesn't need to be refreshed as the bit is latched in it. It can operate at lower supply voltages and has large noise immunity. However, the six transistors of an SRAM cell take more space than a DRAM cell which is made of only 1 transistor and 1 capacitor, thereby increasing the complexity of the cell [3].

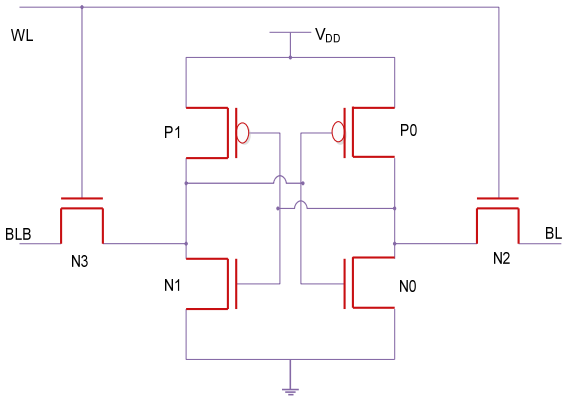

Fig. 1. Conventional 6T-CMOS SRAM Cell [3]

The SRAM memory bit-cell has two CMOS inverters connected back to back (P0, N0, and P1, N1). Two more pass transistors (N3 and N2) are the access transistors controlled by the Word Line (WL), Fig. 1. The cell preserves its one of two possible states "0" or "1", as long as power is available to the bit-cell. Here, Static power dissipation is very small. The

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cell draws current from the power supply only during switching. But in the idle mode, the memory is becoming the main concern in the Deep Sub-Micron (DSM) technology due to its concerns in the leakage power and data retention at lower operating voltages as the size of the cache memory is growing as per the processors generations.

A. The Operation of SRAM Bit-Cell

Although the two nMOS and pMOS transistors of SRAM memory bit-cell form a bi-stable latch, there are mainly the following three states of SRAM memory cell [4], the Write, Read, and Hold states.

B. Data Write Operation

The value to be written is applied to the Bit lines. Thus to write data "0", we assert BL="0", BLB = "1" and to write data "1", the BL = "1", BLB = "0" is asserted when WL="1".

C. Data Read Operation

Read cycle starts with pre-charging BL and BLB to "1", i.e., V_{DD}. Within the memory cell P0 and N1 are ON. Asserting the word line, turns ON the N2 and N3 and the values of Q and QB are transferred to Bit-Lines (BL and BLB). No current flows through N2, thus P0 and N2 pull BL upto V_{DD}, i.e., BL = "1" and BLB discharges through N3 and N1. This voltage difference is sensed and amplified to logic levels by sense amplifiers.

D. Standby Operation (Hold)

When WL = "0", N2 and N3 disconnect the cell from Bit-Lines (BL and BLB). The two cross-coupled inverters formed by P0-N0 and P1-N1 will continue to reinforce each other as long as they are disconnected from the outside world. The current drawn in this state from the power supply is termed as standby current.

III. Leakage Current Mechanism

High leakage current in deep-submicron regimes is the major contributor of power dissipation of CMOS circuits as the device is being scaled. Various leakage mechanisms are show in Fig. 2.

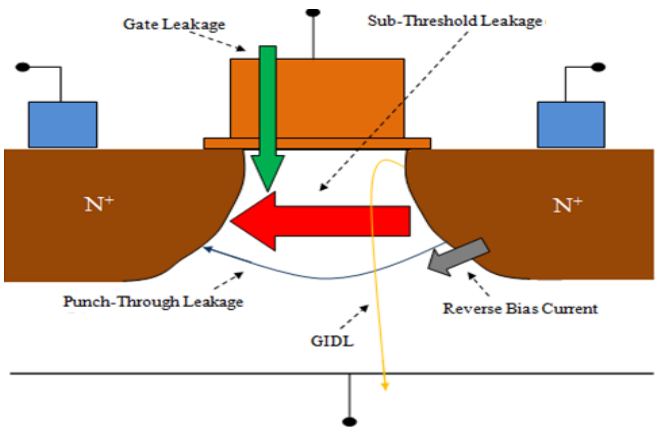

Fig. 2. Leakage current mechanisms of deep-submicron transistors

A. Gate Direct Tunneling Leakage (I_G)

The gate leakage flows from the gate through the "leaky" oxide insulation to the substrate. In oxide layers thicker than 3–4nm, this kind of current results from the Fowler-Nordheim tunneling of electrons into the conduction band of the oxide layer under a high applied electric field across the oxide layer. For lower oxide thicknesses (which are typically found in 0.15µm and lower technology nodes), however, direct tunneling through the silicon oxide layer is the leading effect. Mechanisms for direct tunneling include electron tunneling in the conduction band (ECB), electron tunneling in the valence band (EVB), and hole tunneling in the valence band (HVB), among which ECB is the dominant one. The magnitude of the direct gate tunneling current increases exponentially with the gate oxide thickness t_{ox} and supply voltage V_{DD}. In fact, for relatively thin oxide (in the order of 2-3nm), at a V_{GS} of 1V, every 0.2nm reduction in t_{ox} causes a tenfold increase in I_G [5]. Gate leakage increases with temperature at about 2x/100°C.

B. Sub-Threshold Leakage (I_{SUB})

The Sub-threshold Leakage Current is the drain-to-source leakage current when the transistor is in the OFF mode. This happens when the applied voltage V_{GS} is less than the threshold voltage V_{th} of the transistor, i.e., weak inversion mode. Subthreshold current flows due to the diffusion current of the minority carriers in the channel of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Equation (1) relates the sub-threshold power with other device parameters,

$$P_{Sub-Vt} = \frac{\mu o W_{eff}}{L_{eff}} C_{ox}.V_T^{\,2}.(m-1).e^{(|V_{GS}|-V_{th})/mV_T}.(1-e^{-|V_{DS}|/V_T}) \quad (1)$$

where, $V_T = \frac{KT}{q}$ = 26mV, the Thermal Voltage

P_{Sub-Vt} -Sub-threshold Power, µo –zero bias mobility, W_{eff} – channel effective width, L_{eff}–channel effective length, C_{ox}– Oxide capacitance, V_T- Thermal voltage, V_{GS}- Gate-Source Voltage, V_{DS}- Drain-Source Voltage, K– Boltzmann's Constant, T- Temperature, q – Charge.

As the supply voltage (VDD) is being uniformly scaled down with successive technology nodes. The transistor delay is inversely proportional to the difference of supply and threshold voltage [6], the threshold voltage must also be scaled down proportionally with each technology node to maintain the circuit performance. This leads to an exponential increase in sub-threshold leakage current. Also, increasing the threshold voltage (V_{th}) of the transistor is an effective way to reduce sub-threshold leakage.

C. Effect of Temperature

Temperature dependence of the subthreshold leakage current is important as digital very large scale integrated (VLSI) circuits usually operated at elevated temperatures due to the power dissipation. The variation of the sub-threshold slope with the temperature is shown in Fig. 3 as derived from the sub-threshold model in [10].

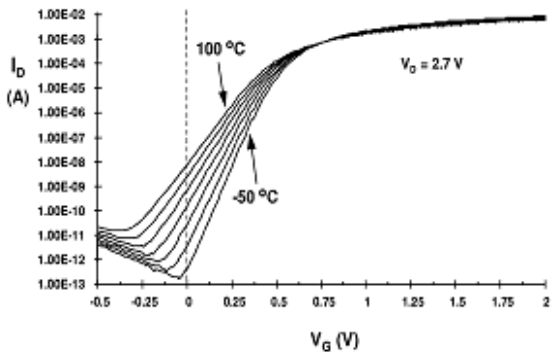

Fig. 3. I_D Vs V_G showing temperature sensitivity of I_{OFF}

C. Reverse-Biased Junction Leakage (I_{REV})

The junction leakage occurs from the source or drain to the substrate through the reverse biased diodes when a transistor is in the OFF state. A reverse-biased pn junction leakage has two main components, one is due to the minority carrier diffusion/drift near the edge of the depletion region and the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction. For Ex: in a CMOS inverter with low input voltage, the nMOS is OFF, the pMOS is ON and the output voltage is high. Subsequently, the drain-to-substrate voltage of the OFF nMOS transistor is equal to the supply voltage (V_{DD}). This results in a leakage current from the drain to the substrate through the reverse-biased diode. If both n and p regions are heavily doped, Band-to-Band Tunneling (BTBT) dominates the pn junction leakage [7]. The junction leakage has a rather high temperature dependency, i.e., around 50–100x/100 ^oC.

D. Direct Gate Oxide Tunneling Current

In very thin oxide layers (less than 3–4 nm), electrons from the inverted silicon surface, instead of tunneling into the conduction band of SiO_2 , directly tunnel to the gate through the forbidden energy gap of the SiO_2 layer [11]. Hence, the direct tunneling occurs at $V_{ox} < \phi_{ox}$ [12]. The equation governing the current density of the direct tunneling is given by [30]

$$J_{DT} = AE_{ox}^2 \exp\left\{-\frac{B\left[1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)^{3/2}\right]}{E_{ox}}\right\} \quad (2)$$

where E_{ox} is the field across the oxide; ϕ_{ox} is the barrier height for electrons in the conduction band; V_{ox} is the voltage drop across the oxide.

IV. A Review of Related Work

In this section, we review some of the previously reported SRAM cell structures.

In [3], a P3 SRAM bit-cell structure at 45nm technology has been proposed for semiconductor memories with high activity factor based applications in Deep Sub-Micron (DSM) CMOS technology, 45nm. It has been proposed for the reduction of the active and the standby leakage power through the gate and sub-threshold leakage reduction in the active and standby mode of the memory operation. The stacking transistor pMOS (P2), connected in series (in line), is kept OFF in standby mode and kept ON in active (read/write) mode. The pMOS transistors are used to lower the gate leakage current [8] while full-supply body-biasing scheme is used to reduce the sub-threshold leakage currents. P3 SRAM bit-cell made a significant fall in dynamic as well as standby powers in comparison to the conventional 6T SRAM bit cell, at the cost of small area penalty and issues with SNM.

In [8], a gate leakage current reduction technique based on the pMOS pass-transistor SRAM bit-cell structure as PP-SRAM cell has been proposed at 45nm technology and 0.8V supply voltage. In this cell, in order to decrease the gate leakage currents of the SRAM bit cell, nMOS pass transistors are replaced by pMOS pass transistors. The use of pMOS lead to performance degradation due to different mobility coefficients for the nMOS and pMOS transistors. To overcome this problem, the width of pMOS pass transistor is selected as 1.8 times of the nMOS. Thus, it has area penalty.

V. Design of IP3-SRAM Bit-Cell

In [9], the IP3 SRAM Bit–Cell structure has been presented which uses drowsy scheme and pMOS stacking with ground, Fig.4. This cell reduces the power consumption (active, leakage, standby) with the small area penalty. The stack transistor is used one per row in the memory array so that area penalty of this transistor can be reduced.

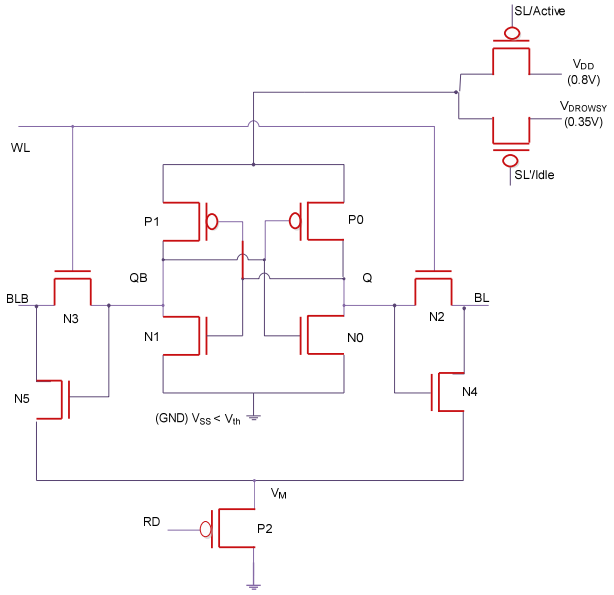

Fig. 4. IP3 SRAM Bit-Cell [9]

Here, all transistors used are of minimum sized transistors except transistor P3 which is about 1.8 times of the nMOS [9].

VI. Simulation and Results

To analyze the gate leakage current and standby power in IP3 SRAM bit cell under temperature variations, the simulation is being performed at Cadence Virtuoso

Environment at 45nm technology using parametric analysis with temperature ranging from -25^{0}C to +125^{0}C.

A. Gate Leakage Current

Fig. 5 shows the variation in gate leakage when the temperature is being varied from -25^{0}C to +125^{0}C. It shows that gate leakage increases approximately exponentially with rise in temperature. Fig. 6 shows the comparative analysis of gate leakage under temperature variations. In IP3 cell, at 125^{0}C, a reduction of 86.11%, 93.2% and 77.6% in gate leakage is observed with respect to 6T, PP and P3 SRAM cells, that is, effect of the temperature variations is least in case of IP3 SRAM cell .

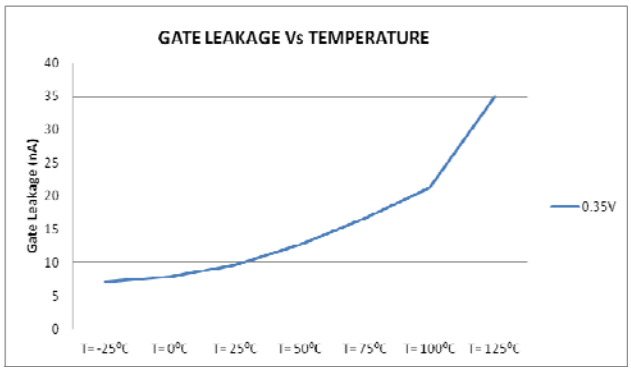

Fig. 5. Gate leakage Vs temperature for IP3 SRAM cell

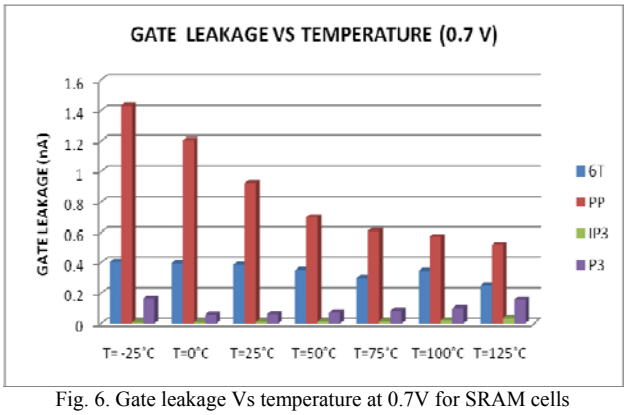

Fig. 6. Gate leakage Vs temperature at 0.7V for SRAM cells

B. Standby Power

Fig. 7 shows the variation in standby power for various SRAM cells when temperature is being varied from -25^{0}C to +125^{0}C. Variation in the standby power is minimum for P3 cell and IP3 cell is at second place for this case.

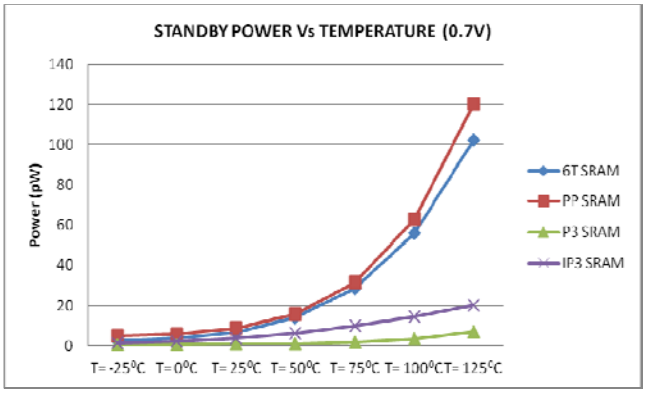

Fig. 7. Standby power for SRAM cells at 0.7V

C. Area

Fig. 8 illustrates the relative comparison of the bit-cell area of the SRAM designs. It is clear that the IP3 cell has the largest area among the 6T, PP, P4, and P3 SRAM cells. The area can be further optimized by layout optimization. The IP3 cell's layout is shown in Fig. 9.

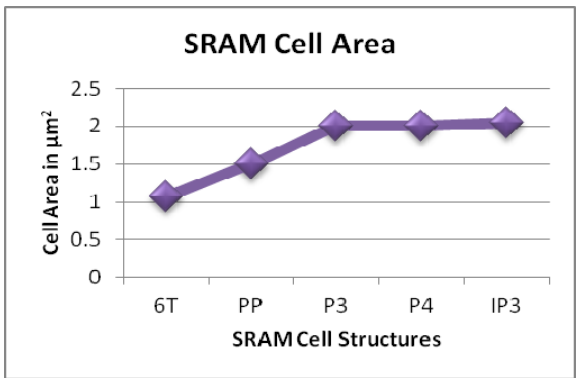

Fig. 8. Chip area comparison

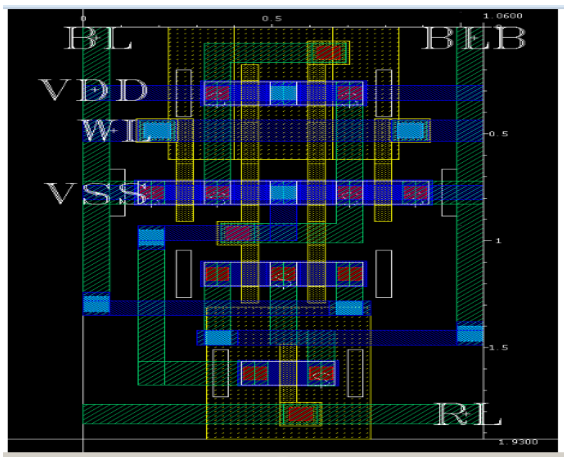

Fig. 9. Layout of the IP3 SRAM Bit-Cell

VII. Conclusion

In this paper, the gate leakage current analysis of the IP3 SRAM cell has been carried out under temperature range -25^{0}C to +125^{0}C and results are compared with 6T, PP and P3 SRAM cells. The gate leakage current variations are the least for the IP3 cell due to the p-MOS stacking effect and the drowsy scheme used in it. As per the simulation results of parametric analysis, leakage current increases with rise in temperature. At V_{DD} = 0.7V, gate leakage reduction of 98.2%, 97.5% and 86% is observed in IP3 cell in comparison with 6T cell at -25^{0}C, 25^{0}C and 125^{0}C temperatures respectively. On making the comparison with PP cell results, gate leakage reduction of 99.5%, 98.95% and 93.2% is observed at respective temperatures. Similarly, comparison drawn with P3 cell results, at the same temperatures, indicates the reduction of 95.6%, 84.7% and 77.6% in gate leakage of IP3 SRAM cell. Standby power leakage is the least for the P3 cell. At 125^{0}C, percentage increase in standby leakage is 80.1%, 83.17% (with respect to 6T, PP cell) if comparison is made with IP3 cell. In IP3 cell standby leakage is more than P3 cell (65.2%). The gate leakage reduction in IP3 cell is achieved on the expense of small area penalty.

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