Design and VLSI Implementation of VCO for High Speed RF Applications

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Abstract—**Voltage-Controlled Ring Oscillators are crucial components in many wireless communication systems. VCRO is used in PLL circuit, used to generate the oscillations and increase the speed of the whole system for RF wireless communication such as 60GHz communication systems. This kind of VCRO used in high-resolution oscillators for different applications. The goal of this project was to design a high speed, low power and minimum cell area, Voltage-Controlled Ring Oscillator in CMOS 0.18 micron technology that makes it suitable for wireless application. Designing of particular VCRO there are nine differential amplifier stages in cascading with each other and the output of last stage is again feedback to the input of the first stage. First according to the specification, the design of aspect ratio of the transistors used in our design is done. There were many challenges throughout the design process, including determining the matching requirements of the devices, investigating what percentage of segmentation to be used to design the whole system. For checking the functionality of the whole system a spice code is written using H-Spice by defining all blocks in the circuit as sub circuits, which are delay cell, bias and tuning circuitry. Then a schematic capture is done using schematic composer from virtuoso stating from bottom level to top level.**

Index Terms—**Ring based Voltage-Controlled Oscillator (VCO), Differential Amplifier(DA)**

I. INTRODUCTION

The specifications are to design a voltage-controlled oscillator (VCO) based on ring oscillators, which provides a frequency range from 1.884GHz to 1.9GHz [1, 2, 3]. The voltage applied to the VCO is 1.8V. The power consumption of the whole oscillator should not exceed 27mW. The overall objective is to design a robust VCO with minimum power consumption and minimum consumed cell area. The design of the VCO must be in 0.18um CMOS technology, and include delay cells, bias circuitry, and tuning circuitry.

Fig. 1. Differential Ring Oscillator [4]

Ring oscillator structure also employs positive feedback to achieve oscillation [5, 6, 7]. The above circuit depicts an N-stage ring oscillator realized using differential cells, which have complementary outputs. A source coupled pair inverter

will be typical implementation. Denoting t_p as the propagation delay through each stage, then period T = $2Nt_p$.for a single-ended output cell, N has to be odd, but for differential cell N can be odd/even, to start an oscillation. Assuming that 180^0 of phase shift is provided by the chain of N stages, each stage must provide $180^0/N$ of phase shift and sufficient gain at w_0.

Fig. 2. Fundamental Frequency

A saturated delay cell is required to generate a large oscillating voltage swing, while using a low voltage rail of 1.8V. Hence, the slow-slewing saturated delay cell. Below was chosen, over its more complicated fast-slewing counterpart. The overall architecture consisting of the bias circuitry, delay cell, and tuning circuit.

II. DESIGN OF DELAY CELL

We will design the VCO to consume 27mW, to allow for extra performance and margin from the specified 54mW [4]. Using the formula for power specification,

$$Power = N \times I_{bias} \times V_{dd} = 9 \times I_{bias} \times 1.8V = 27mW \quad (1)$$

We obtain

$$I_{bias} = 1.6667\,mA.$$

The voltage swing of the oscillator is determined by the resistance of M3 biased in the triode region. We wish to obtain a swing of 1V. Hence, the equivalent resistance required is given by,

$$RM_3 = \frac{V_{swing}}{I_{bias}} = \frac{1V}{1.6667\,mA} = 600\Omega \quad (2)$$

Fig.3. Slow-slewing Saturated Delay Cell

Now, we can determine the size ratio (W/L)3 of M3. Since M3 is to be biased in triode, we use the triode equation

$$RM_3 = \cfrac{1}{kp\left(\cfrac{W_3}{L_3}\right)\left(|V_{gs3}| - |V_{tp}| - |V_{ds3|}\right)} \quad (3)$$

VGS3 must be high to bias M3 in deep triode, hence, an initial value of |VGS3| = 1.2V is chosen. When M3 is biased at the midpoint of the Vds3 vs. Id3 curve,

|VDS3| = Vswing/2 = 0.5V.

Substituting all values in the above equation, we obtain (W/L)3 = (12.371um/0.18um)

The frequency of the VCO depends on the width of the source coupled pair, M1 and M2 of the delay cell. In general,

$$f_o = \frac{1}{2Ntp}, \text{ where } tp = RCl \times ln2$$

Cl is the loading capacitance, and its value depends on the size of the source coupled pair in the current delay cell, the size of the SC pair in the next delay cell, and the size of the triode-biased PMOS, M3.

$$Cl = \frac{1}{2NRfoln2} = \frac{1}{2 \times 31.9GHz \times 600\Omega \times ln2} = 0.21092pF$$

Since the size of the SC pair in the next delay cell dominates the contribution to Cl, we will approximate Cl=Cgs (M1) as an initial approximation.

Cgs(M1) = W1 x L1 x Cox = W1 x 0.18um x 8.445x10^{-3} = 0.21092pF.

Hence, (W1/L1) = (138.59um/0.18um)

III. DESIGN OF BIAS CIRCUITRY

A replica bias scheme is implemented to maintain a constant Vswing. Although the design of a replica bias is more complicated than a constant bias scheme, the use of a replica bias allows the VCO to be less susceptible to process variations, noise on the power supply, and temperature variations. This is accomplished by designing PBIAS to fluctuate correspondingly with Id of M3, and NBIAS to fluctuate correspondingly with Ibias. In other words, a replica bias ensures the voltage drop across M3 and M4, and the voltage drop across the current source to remain at a constant, despite fluctuations in Itail. Since 6 the VCO is designed to operate at a high frequency within a narrow frequency range, a replica bias is essential for a robust design. Since a low voltage rail of 1.8V is used, we are unable to design a cascoded NMOS current source in the delay cell. Hence, we have only used one NMOS to create a current source. The approximations and hand calculations used in designing the bias circuitry are

Since we know M3 must be in deep triode, we set Vgs9 = 1.15V much larger than Vgs14=0.55V, which is just enough to turn M14 on. Hence,

R = 180.18Ω

Vov9 = Vgs9 – Vtp = 1.15V – 0.437V = 0.713V

Vov14 = Vgs14 – Vtn = 0.55V – 0.445V = 0.105V = Vov6

M14, M9, and M6 must be in saturation. Hence, we can use the following formulas to determine the size of all three transistors.

$$\frac{Ibias}{2} = Kn\left(\frac{W}{L}\right)_{14} V^2_{0v14}$$

$$\frac{Ibias}{2} = Kp\left(\frac{W}{L}\right)_{9} V^2_{0v9}$$

$$I_{bias} = Kn\left(\frac{W}{L}\right)_{6} V^2_{0v6}$$

The calculated sizes are (W/L)14 = (70.137um/0.18um), (W/L)9 = (6.4um/0.18um), and (W/L)6 = (140.21um/0.18um). Note that the sizes of M14 and M6 are especially large in order to keep both transistors in saturation with a low Vgs of 0.55V.

Hence, the PBIAS = Vdd – Vgs9 = 1.8V – 1.15V = 0.65V and NBIAS = Vgs14 = 0.55V.
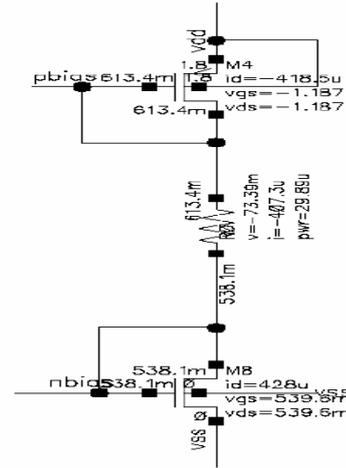
Fig. 4. Circuit Diagram of Bias Circuitry

IV. DESIGN OF TUNING CIRCUITRY

We chose Vtune_max = 1V and Vtune_min = 0V for ease of use. The corresponding gain of the VCO is given by

$$K_{VCO} = \frac{df_o}{dV_{tune}} = \frac{f_{max} - f_{min}}{V_{tune\,min} - V_{tune\,max}} = \frac{1.9GHz - 1.884GHz}{0V - 1V} = -16MHz/V$$

To build a safety margin, we set Kvco = - 22MHz/V. The size of M7 and M8 can be determined by the following relation

$$GM_{7-8} = \frac{K_{VCO} \times \left(|V_{GS3}| - |V_{tp}| - |V_{DS3}|\right)}{-f_o \times R_{M3}} = 16.6544uA/V$$

Hence,

Itune_max = 16.65uA/V x 1V = 16.65uA

Since Itune_bias must be larger than Itune_max, we set Itune_bias = 20uA.

Finally, to determine the size of M7 and M8,

$$GM_{7-8} = \sqrt{I_{tune\_bias} \times \left(\frac{W}{L}\right)_7} = 16.6544uA/V$$

(W/L)7 = 0.1504 = (0.027um/0.18um)

However, the minimum width allowed for 0.18um technology is 0.3um. Hence, we will scale W7 up by a factor of 10, and adjust the gain of the current mirror M11 to M12 to obtain the correct Itune_bias.

Since M7 and M8 were scaled by a factor of 10, we must scale Itune_bias also by a factor of 10, and design 10(W/L)11= (W/L)11 to obtain the appropriate Itune. The

size of the PMOS current source of the tuning circuit is obtained by

$$I_{tune\_bias} = \frac{K_p}{2}\left(\frac{W}{L}\right)_{Ptune\_bias}(|V_{gs}| - |V_{tp}|)^2$$

where Itune_bias = 10 x 20uA = 200uA, |Vgs| = |PBIAS-Vdd| = |0.65V – 1.8V| = 1.15V. Therefore, (W/L)Ptune_bias = (1.53um /0.18um). For M11 and M12, we arbitrarily choose (W/L)11 = 0.3um and (W/L)12 = 3um.
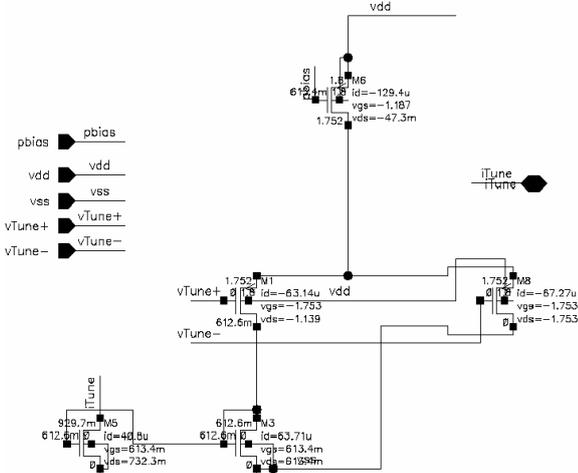
Fig.5. Circuit diagram of tuning circuitry

V. CIRCUIT IMPLEMENTATION

The calculated sizes summarized in Table 2 are used in our initial simulation. However, we made significant modifications based on parametric simulation results. The modifications made and the actual implementation of the VCO is discussed in this section of the report. Figure 2 shows the schematic of the VCO in Cadence. According to the previous section, the VCO is composed of three delay cells, a bias block, and a tuning block.
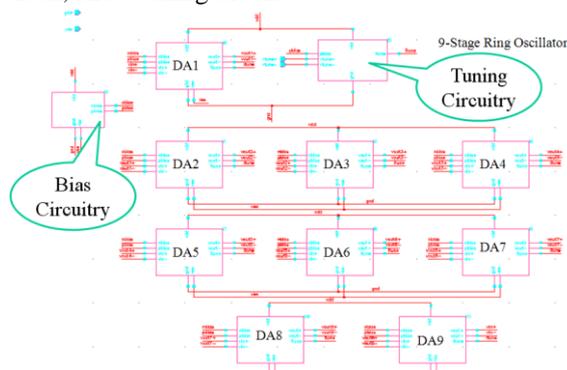
Fig. 6. 9-Stage Ring Oscillator

The above circuit is the 9-stage ring oscillator, which consist of 9-delay cells , bias circuitry, and tuning circuitry. The interconnection of all 9-stages are cascaded to each other and feedback to the input of the first delay cell so that by tuning the tuning voltage, we can get the required oscillations of frequency is 1.9GHz.

VI. PRE-LAYOUT SIMULATION

The designed VCRO has to work according to its functionality. After the generation of net-list of SPICE the simulation results are produced by using H-SPICE. We add all the required input voltages such as tuning and bias voltage. The power supply is given as 1.8V. For simulation we used the standard termination resistance 180.2 ohms. The total power dissipation of the entire VCRO is also calculated using H-SPICE. The differential waveform (Vout+ - Vout-) of the VCO output, and shows the gain and phase shift of Vout+ and Vout- waveforms. The voltage swing is almost 1V, as designed.
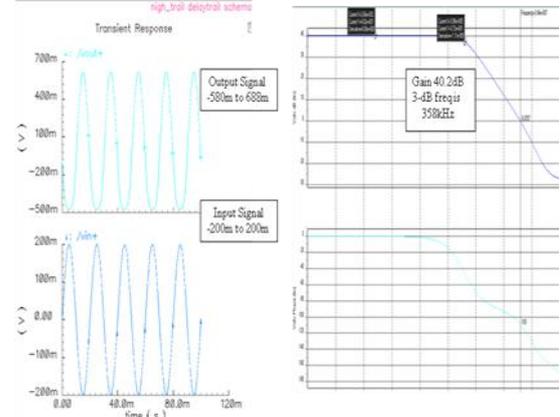
Fig.7. Simulation results of Differential Amplifier

Fig.7. shows the transfer characteristic that shows the functionality of the Differential Amplifier. The desired output voltage swing is obtained as -1 to 1V. In the above graph x-axis showing the time and y axis represent the voltage. The two graphs show the transient and AC response outputs. For the transient response the voltage swing is between -1 to 1V and AC response of differential amplifier given that gain of 53dB.

The frequency of oscillation and the performance of the tuning circuit was thoroughly described. In summary, the frequency of oscillation with Vtune+ = Vtune- = 0V is 1.9001GHz and with Vtune+ = 0.9V and Vtune- = 0V is 1.884GHz. The voltage swing is unchanged as the frequency changes from 1.884GHz to 1.9GHz.

First current output labelled as Ion in figure 5.1 gives minimum current for all zero bits and maximum current for all one bits. The second current output Iop in figure 5.1 gives a maximum current for all zero bits and minimum current for all one bits. The two current outputs always show a change with respect to the change in the corresponding digital inputs.

A. Pre Layout Simulation of VCRO
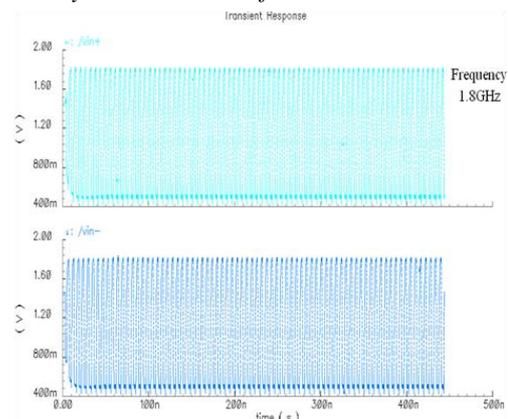
Fig. 8. Pre Layout Simulation of VCRO

The Fig.8. shows the simulation result of 9-stage ring

oscillator, which produces the frequency of range 1.884GHz to 1.9GHz. The frequency of oscillation and the performance of the tuning circuit was thoroughly described.

The layout of VCRO is drawn using Layout-XL and cleared the extraction warnings, errors. The problem getting while doing the layout is the metals spacing, sizing of metals. The nmner of metals used are 3-metals to designed the whole voltage controlled ring oscillator.

Fig. 9. Layout of VCRO

The layout of VCRO is drawn using Layout-XL and cleared the extraction warnings, errors. The problem getting while doing the layout is the metals spacing, sizing of metals. The nmner of metals used are 3-metals to designed the whole voltage controlled ring oscillator.

Both DRC and LVS of the VCRO layout is done using Assura. In this, it compares the schematic and layout. The comparision between the pins mismatch, nets mismatch, devices mismatch.

Actually, pre-layout simulation does the functionality and it would not consider the parasitic. So that in post layout simulation considering the parasitic, the delay between the input to output would increased because of the parasitic. The above figure shows the Assura RCX run LVS completed successfully.
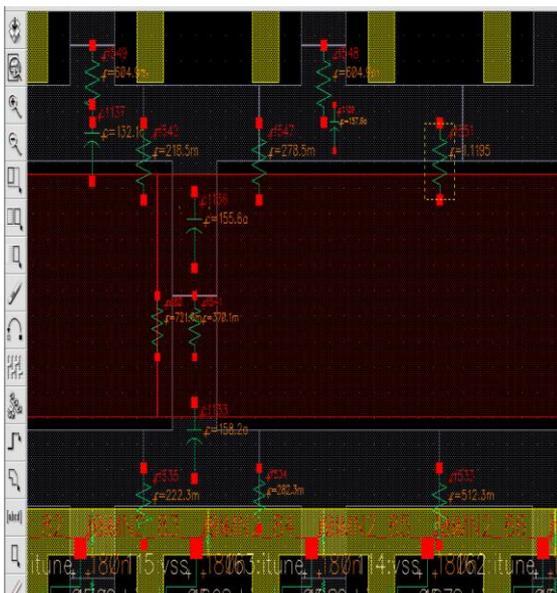
Fig.10. shows the extracted view of R & C

B. Power Consumption

One of our main aims is to reduce the total power consumed by the whole design by reducing the total power consumption from the analog part as the power consumption at the digital decoder is usually negligible due to dynamic nature of the CMOS logic cells.

C. Comments

The total power consumed by the VCRO is evident from the figure that the VCRO consumes a maximum power of 27mW. In the above graph, X-axis showing time and Y-axis shows the total Voltage swing. In this design, power supply of 1.8V is selected.

D. Layout

Much of the layout for the VCRO was straight forward. The tool virtuoso XL is used for the layout purposes. First the basic differential amplifier, bias circuitry and tuning circuitry are drawn. Then place and route for these cells was performed by hand to complete the whole layout. These blocks, which has cascaded 9-stages of differential amplifiers, were also laid out with the intent of having equal spacing between the outputs, allowing for easy connection to the VCRO. To minimize the area, a full custom design was performed.

The layout of the cell measures 35.72m x 29.80um. To save time, we utilized the readymade transistor from the CMCpcells library to layout the circuit. We originally intended to use poly resistors to layout the resistance of 180.2Ω in the bias circuitry. However, the resistance is too low for a poly resistor, and we resolved to use an N-implant resistor, due to its lower sheet resistance. In additions, this layout utilizes two metal layers to provide connections to the metal contacts. As for body contact sharing, all transistors require a connection to a voltage biased body contact. For PMOS transistors, the body is of N-type and connected to VDD. For NMOS transistor, the body is of P-type and grounded. DRC allows transistors to share a body contact as long as the contact is within 5 µm from the body. Hence, we can reduce the number of body contacts in the layout by sharing between transistors. The following is an excerpt from the built-in DRC test in Cadence. The excerpt shows that our layout has successfully passed the DRC test.
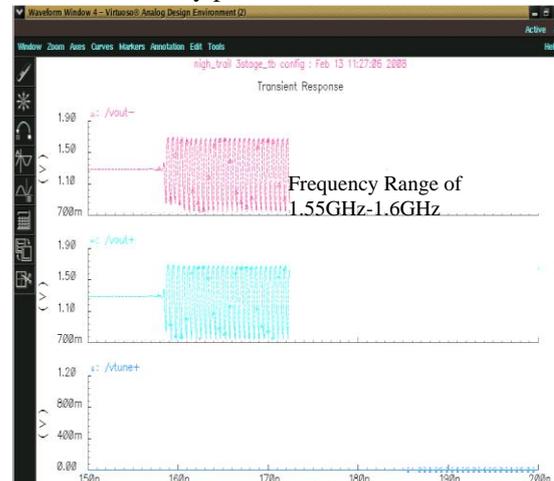
Fig.11. Post-Layout Simulation Result of VCRO

VII. CONCLUSION

The design of our Voltage Controlled Oscillator (VCO) was implemented using a 9-stage ring oscillator. A slow-slewing saturated topology was used for all nine delay cells of the ring oscillator. From circuit simulations, the oscillating voltage swing is close to 1V. The output frequency varies from 1.884GHz to 1.9GHz by adjusting the tuning voltage from 0.9V to 0V. Therefore, the simulated K_{VCO} is -17.9MHz/V, which is very close to the calculated value of -16MHz/V. The power consumption is of the VCO is 3.2mW at 1.9GHz, and the total consumed cell area is 35.72m*29.80um. Therefore, we have met or exceeded all project specifications.

The goals of this project are concluded in this chapter. First, different VCRO architectures were analyzed to determine the optimal topology for the given performance specifications with minimum power consumption. Second, the exact implementation of the chosen architecture was investigated in an effort to use the minimum amount of power. Due to some limitations the speed of the designed 9-stage VCRO cannot able to be measured. After a complete analysis, the block was simulated for functionality verification. Once confirmation of correct operation was achieved, a complete layout was done in order to optimize the area.

Simulation results from Spice demonstrate that the VCRO achieves all required performance specifications in terms of accuracy and performance parameters such as minimum cell area and minimum power. The measured phase margin >55 degree and gain 100v/v. Finally, there should be no problems with accuracy as the current source transistors were sized in such a way that matching would not be a problem.

ACKNOWLEDGMENT

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