

A Class AB Amplifier with a Reduced Crossover Distortion for Signal Driver

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Abstract—A high-driving class-AB buffer amplifier, which consists of a high-gain input stage and a pair of operational transconductance amplifier, is proposed. This paper presents a novel systematic offset minimization. The high-driving capability is mainly provided by the folded amplifier class-AB CMOS operational amplifier. The proposed structure has a replica-gain circuit, generating a dc replica bias to the differential input stage, and providing differential gain as well as level conversion to drive the class- AB output stage. The circuit contains transconductance amplifiers in a rail to rail operation with both input and output stage based on the microwind technology and the offset due to device mismatch. An op amp low Cmos design is present in this paper. The circuit uses dual transconductance input pairs to achieve a rail-to-rail common mode input voltage range. Special attention has been given to the offset voltage cancellation of the op amps., and the circuit exhibits the settling time of 3 μ s, for a voltage swing of 3.3 V under a 560pF capacitance load with a power supply of 5 V. The offset voltage of the amplifier reduced to a very small value of 0.0182mv. The area of this amplifier is 40*70 μ m².

Index Terms—CMOS, multistage amplifiers ,class-AB amplifier, signal driver, offset voltage cancellation, , operational transconductance amplifiers (OTAs)

I. INTRODUCTION

A signal driver like LCDs are previously installed in notebook type personal computers and compact desktop personal computers and monitors are becoming larger and higher definition, there is a big demand of developing low power dissipation, high resolution, small settling time and high-speed signal driver . An LCD driver is generally composed of column drivers, gate drivers, a timing controller, and a reference source. The column drivers are especially important to achieving high-speed driving, high resolution and low-power dissipation. Class A and class B amplifier combine their configuration in class AB amplifier in which small collector current will flow when there is no input signal but it is much less than that for the Class A amplifier . This means then that the transistor will be "ON" for more than half a cycle of the waveform but much less than a full cycle. The amount of diode biasing voltage present at the base terminal of the transistor can also be increased in multiples by adding additional diodes in series[1]. Constructional Imperfection of the devices causes an offset voltage, which limits the high-resolution for signal deriver driver application. Previously circuits are proposed for the offset voltage

cancellation. like, "output offset storage" and "input offset storage" techniques measure the offset voltage and store the charge on capacitors in series with the output and input. However, these two techniques introduce capacitors in the signal path, a particularly serious issue in op-amps and feedback system. To resolve the above Issues, an offset cancellation scheme, which can isolate the signal path from the offset storage capacitors through the use of an auxiliary amplifier, was proposed. A push-pull stage is often used as an output stage in CMOS buffer amplifiers. The push-pull stage consists of two complementary Common-source transistors, allowing rail-to-rail output voltage Swing. The classes AB Amplifiers for signal Driver applications have been proposed in previously work[4], in which the number of current path is reduced and the phase Compensation is suitable for fast speed of operation. No more current paths are needed for the class-AB operation, this amplifier consumes less current and occupies smaller die area. A high-speed low-power class-AB buffer Amplifier with reduced cross over distortion, which is suitable for signal driver applications, is proposed. The summing circuit is biased by the constant current sources to applicable different supply voltages. The buffer draws little current while static but has a large driving capability while transient. The circuit achieves the large driving capability by employing simple comparators to sense the transients of the input to turn on the output stages, which are statically off in the stable state[10]. This increases the speed of operation of the circuit without increasing static power consumption. An experimental prototype output offset voltage is 0.0182mv buffer implemented in a 90nm CMOS technology demonstrates that the circuit can operate under a wide power supply range. Quiescent currents

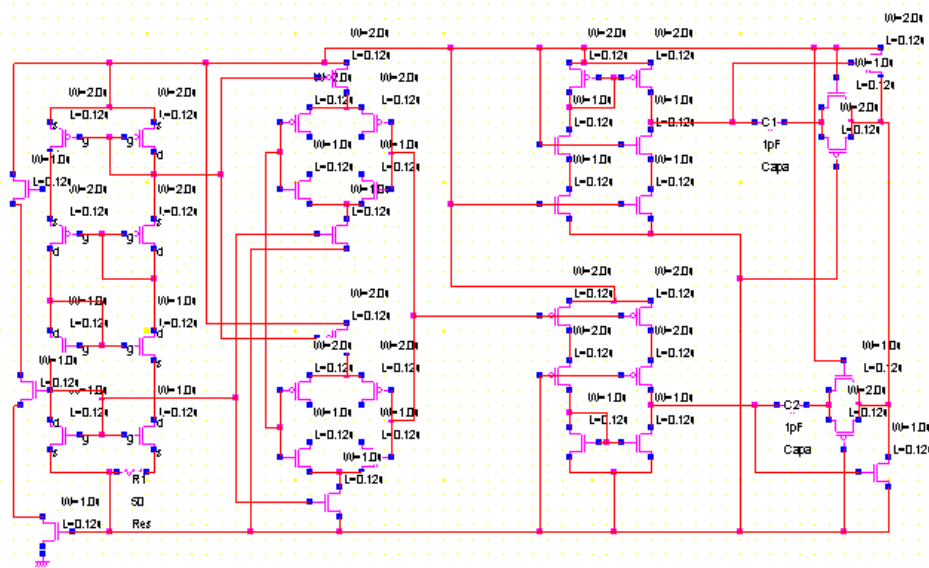


Fig. No 1(a) proposed Circuit Without Offset Cancellation

II. PROPOSED CIRCUIT WITHOUT OFFSET CANCELLATION

The proposed offset cancellation circuit contains the proposed two-stage buffer amplifier, shown in Fig. 1, consists of 1) four transconductance amplifiers, TCA1, TCA2, TCA3, and TCA4, 2) two transimpedance amplifiers, R1 and R2; and 3) a pair of common-source amplifiers, A20 and A21. The four transconductance amplifiers are dual complementary differential pairs, which, along with the two transimpedance amplifiers, [2] compose the first stage. TCA1 and TCA3 are main transconductance amplifiers, and TCA2 and TCA4 are auxiliary transconductance amplifiers. TCA1 and TCA3, which are NMOS input and PMOS input differential pairs, are actively loaded by R1, while TCA2 and TCA4 are actively loaded by R2. The complementary Common-source amplifiers, A20 and A21, are used to design the signal driver [5]. The dual- input and single-output amplifier incorporates a complementary

The CMOS transconductance and transimpedance amplifiers form the first stage, in which the transimpedance amplifiers added the currents of the main and auxiliary transconductance amplifiers to achieve the complementary input operation. of 5 μ A and. The buffer exhibits the settling time of 3 μ s for a voltage swing of 5 v under a 560 pF capacitance load. The area of this buffer is 40*70 μ m².high and middle level signals. The proposed amplifier with compensation resistors for low , high and middle input levels, respectively. The simulated phase margins of the amplifier without compensation resistors for low, high and middle input levels are calculated. They can be seen that the amplifier has a large enough phase margin for driving a large load even without the compensation resistors. However, the compensation resistors are needed to improve the stability for a small load. In this configuration of the proposed class AB transconductance amplifier[3]. As a buffer, low-resolution driver ICs does not employ the offset cancellation technique. However, this technique is recommended in high-quality signal driver Amplifiers without and with offset cancellation is described in the fig1 (a), (b)

III. RAIL-TO-RAIL OPERATION

The offset voltage cancellation circuit operation requires rail to rail input pairs. The rail-to-rail operation requires complementary input pairs. The difference in random offset voltages of these input pairs translates into a global offset with nonlinear variation over the common mode input range. This nonlinear offset is one of the main causes of large signal distortion in rail-to-rail circuits. To take full advantage of an input range that can exceed the supply, at a single 3.3 V supply. The main and auxiliary transconductance amplifiers are dual complementary differential pairs; thus, when the input voltage is near to rail voltages, one of the main transconductance amplifiers is cut off although its counterpart auxiliary transconductance amplifier still operates. The difference in random offset voltages of these input pairs translates into a global offset with nonlinear variation over the common mode input range [6]. This nonlinear offset is one of the main causes of large signal distortion in rail-to-rail circuits[5]. To take full advantage of an input range that can exceed the supply, at a single 3V supply. The main and auxiliary transconductance amplifiers are dual complementary differential pairs; thus, when the input voltage is near 3V [8] , one of the main transconductance amplifiers is cut off although its counterpart auxiliary transconductance amplifier still operates. For example, as the input voltage is near to the value of VDD, Gmp and Gmap are cut off, but Gmn and Gman can amplify the input signal to the output stage through R1 and R2, respectively This has the benefit of overcome crossover in servo systems and reduces distortion component. When the input common mode range goes below 2V above the negative rail, the NPN input pair (T1, T2) cut off and the PNP input pair[7]. The circuit representation and block diagram of the proposed amplifier are illustrated in Figure 2 [b]. The offset voltage cancellation, input bias current, voltage noise and bandwidth are also degraded.

Transconductance Amplifier

$$I_{o1} = V_{in1}g_m$$

$$I_{o2} = V_{in2}g_m$$

Transimpedance Amplifier

$$V_{O1} = I_{in1}g_v$$

$$V_{O2} = I_{in2}g_v$$

As the input voltage is at the High level

$$g_{m1} = TCA_1 + TCA_3$$

As the input voltage is at the middle level

$$g_{m1} = TCA_1 + TCA_2 + TCA_3 + TCA_4$$

As the input voltage is at the low level

$$g_{m1} = TCA_2 + TCA_4$$

$$I_D = \mu_n \cdot C_{ox} \cdot W [2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2] / 2L$$

$$I_D = K_n \cdot [2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

for $V_{GS} \geq V_T$ and $V_{DS} < V_{GS} - V_T$ The symbolic representation and block diagram of the instrumentation amplifier are illustrated in Figure 1. It consists of a couple of G,-elements as input stage followed by a unity voltage-gain output stage. Ideal matching between G,-elements, differential voltages $v_{il} = (v_{i1} - v_{i2})$ and $v_{iz} = (v_{ipz} v_{i2})$ produce small-signal currents

$$i_1 = g_m (v_{i1} + v_{i2}), i_2 = -g_m (v_{i1} + v_{i2})$$

where g_m is the input-stage transconductance. Mirrored by a factor B, these currents are summed up at the G,-stage output yielding a small-signal voltage $VO^* = B g_m r_o (v_{i1} + v_{i2})$

Where r_o is the G,-stage output resistance. It is assumed that no current flows into/from the output Stage. Considering a perfectly linear G,-stage, Where A_{b1}, A_{m1} are the amplifier low-frequency.

IV. PROPOSED CIRCUIT WITH OFFSET CANCELLATION

The four transconductance amplifiers are used to extend the input swing. They can also be used for the offset cancellation[10]. The construction layout of the proposed circuit with an offset cancellation is shown in Fig.3, where an offset storage capacitor and three switches are used in the circuit, $V_{OS1}, V_{OS2}, V_{OS3}, V_{OS4}$ are the input-referred offset voltages of TCA1, TCA2, TCA3, and TCA4, respectively. Since the input stage contains both PMOS and NMOS The schematic circuit is depicted in Fig. 1, which is divided into four parts: differential input stage, replica-gain stage, class-AB output stage and biasing stage. Transistors M1, M2, M4, M5 and M7 constitute the basic differential input stage. The replica-gain stage consists of a replica-biasing generator and a full differential amplifier. The replica biasing generator, which is the half circuit of the input stage, is made up of transistors M3, M6 and M9. Due to identical biasing current level in the replica generator, the trackings as well as matching characteristics are excellent. It should be noticed

that the reference input V_{re} of the amplifier is tied to the analog ground because the input terminals of the operational amplifier are forced to analog ground potential under feedback mechanism at quiescent condition* In addition, the fully differential amplifier consists of transistors M11, M12, M13, M14 and M8. It serves dual functions as where are the respective transconductance.

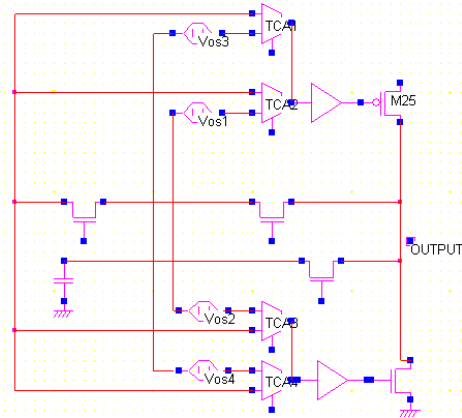


Fig.2(a) proposed circuit with reduced offset

Differential amplifiers, the offsets' voltage varies with the input voltage. The operation is divided into offset cancellation and driving phases[11]. Before each driving phase, the amplifier is in the Non-inverting input terminal (in+). The data line of the signal Driver is connected to the output labeled "out". When the non-inverting input voltage, v_{in+} , is reduced, the gate voltages of A20 and A21 are offset cancellation phase, the switches MOS2 and MOS3 are turned on, and the switch MOS1 is turned off. After the offset cancellation is finished, MOS1 is turned on and MOS2 and MOS3 are turned off. The circuit is then ready to drive its load During the offset cancellation phase, a negative feedback loop consisting of the auxiliary transconductance amplifiers, TCA3 and TCA4, the transimpedance amplifiers, R1 and R2, and the output transistors, A20 and A21[8], is formed. The input voltage is applied to the inverting input terminals of all transconductance amplifiers and to the non-inverting input terminals of the two main transconductance amplifier amplifiers offsets contains both PMOS and NMOS differential amplifiers, the offset is ready to drive its load, After the offset cancellation is finished, MOS1 is turned on and MOS2 and MOS3 are turned off. The circuit is then ready to drive its load contains both PMOS and NMOS differential amplifiers, the offset amplifiers, the offset contains both PMOS and NMOS differential amplifiers.

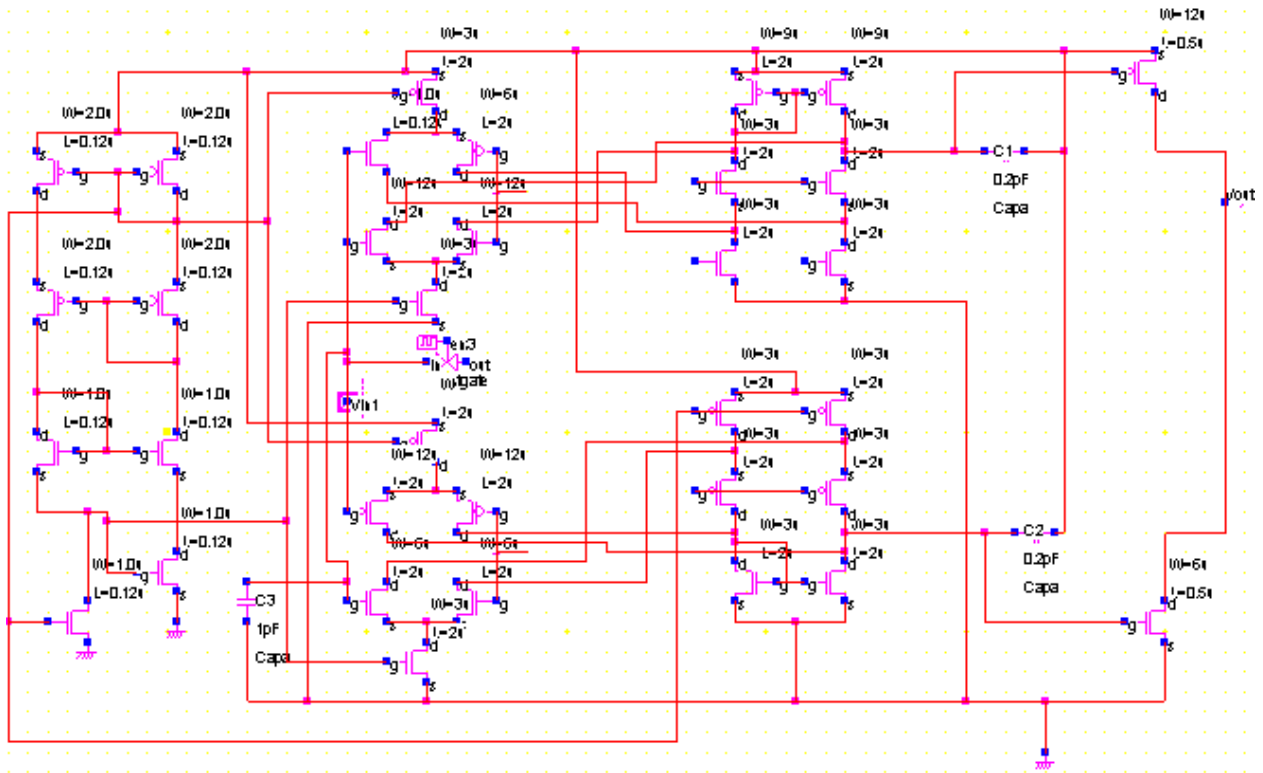


Fig.1(b) Circuit With Offset cancellation

Increased. As a result, M21 starts to discharge the output node. When the output voltage reaches thlevel that the voltage difference between the input and output is almost zero, A20 stops discharging the output node. Similarly, when the input voltage, in , is increased, A21 charges the output load until the output voltage almost equals to the input voltage.

V. CIRCUIT DESCRIPTION

In the stable state, the output voltage is equal to the input voltage. The currents flowing in all transistors of the differential pairs are I where I is the current flowing in the bias stage. The currents flowing in the constant current sources of M9~M12 are also I . Then the currents flowing in M13~M14 and M19~M20 have twice the current in the bias stage, i.e., $2I$. Since M13~M20 are two cascode current mirrors, the drain voltage of M14 is equal to that of M13 and the drain voltage of M20 is equal to that of M19. The currents flowing in the current mirrors are mirrored to the comparators. The aspect ratio of M21 is designed to be smaller than half that of M14 and the W/L of M22 is larger than half that of M20, this causes M21 to be in the saturation region but M22 to go out of the saturation region and be in the triode region. The offsets are stored on capacitors C(s) respectively. The four clock phases are generated on chip with an interlocked logic design. This approach guaranties the correct phase sequencing and no overlapping intervals between phases on the order of two gates minimize the systematic offset voltage. Furthermore, the unity gain amplifiers have been dimensioned in such a way that the overall amplifier gain is unity for positive and negative out output voltages amplifier gain is unity the charge injection

on the offset capacitors and the clock feed through has been minimized by reducing the skew between the PMOS and the NMOS [7], [8]. Dynamic operation current loss is another unnecessary use of current from the supply voltage during the charging and discharging of the display panel. In principle, the total charges provided by the supply voltage Should be equal to the sum of the charges consumed in the amplifier during the steady state and the charges transferred to the display panel load during dynamic operation. In this case, the current consumption of a buffer amplifier during the or discharging operation is larger than that of the steady state, especially when the amplifier has feedback loops to enhance the slew rate [2], [7].

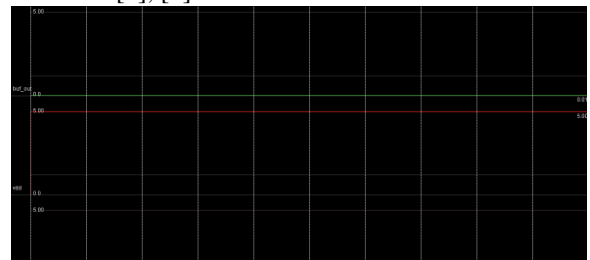


Fig.3(a) output waveform with offset cancellation

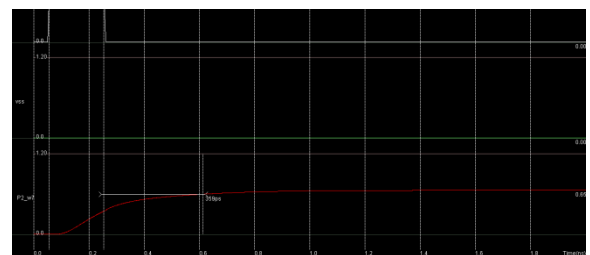


Fig.3(b) output waveform of settling time

VI. CONCLUSION

The proposed buffer amplifier of fig1(a) and (b) were fabricated using 90nm cmos technology. The average active area of one figure is $40 \times 70 \mu\text{m}^2$. The proposed two circuits are measured with a power supply of 3.3V and a large capacitor load of 560pf, offset cancelling technology is used, which is suitable for high resolution Signal drivers. Offset voltages due to constructional imperfection are highly reduced. The settling times for the first circuit to settle to within 0.2 % of the final voltage are $3 \mu\text{s}$ and $2 \mu\text{s}$ for rising and falling edges, respectively. However, the settling times for the improved circuits are $2.4 \mu\text{s}$. The offset voltage of the amplifier with offset cancellation is 0.0128 mV, the active area of this amplifier is $40 \times 70 \mu\text{m}^2$. The measured data shows that the proposed amplifier is very suitable for high color depth and high-resolution signal drivers.

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