Design of Frequency Discriminator for Ringer using 0.18 μm CMOS Technology

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Abstract— **Ring frequency discriminator is an electronic system that can check the frequency of any incoming signal whether it is in the frequency band or not. It is also one of the features for CMOS Speech and Ringer integrated circuit (IC) that can perform all the necessary speech and line interface functions for telephone sets. The signal is considered as a valid signal if it has frequencies between 20 Hz and 60 Hz (20 Hz < ring frequencies < 60 Hz). For future work, it is also possible to design a ring melody generator. Once the valid ring signal is detected and is present for about 75 ms (depends on the designer) continuously, the melody generator will be activated, the ring signal will be monitored continuously and the melody generator will be immediately turn on or off according to the momentary presence of a valid or invalid ring signal respectively until next power on reset or off-hook. This work is implemented using Silterra 0.18 μm CMOS technology.**

Index Terms—**integrated Circuit, Ringer, CMOS**

I. INTRODUCTION

Ringer is the mechanism in a telephone that announces an incoming call. The most problematic is that how to get telephone ringing when there is an incoming call. The electronic ringing circuits are normally not sensitive to the ringing voltage and they must ring with ring signal frequencies between 20 Hz and 60 Hz [1]. The purposed frequency architecture (see Fig. 1) has clipping operational amplifier, NAND gate, J-K flip-flops, and synchronous binary counter. All of these circuits will be designed up to transistor level. The method for determining frequency range is implemented using a counter. The counter is used to divide a certain clock signal. The output of counter with different frequency can be 'edited' with some logic gates to determine the frequency of the incoming signal.

II. METHODOLOGY

A ring frequency discriminator will receive a sinusoidal ringing signal. With a clock pulse applying to the counter, then enable the counter to count clock pulses within a cycle of ringing signal. With the given applying clock pulses count on the counter, frequency characteristic of the ringing signal can be distinguished. A ring detector is required to react to any signal of at least certain amplitude within the frequency band of 23 and 54 Hz as a true ringing signal, and outside of
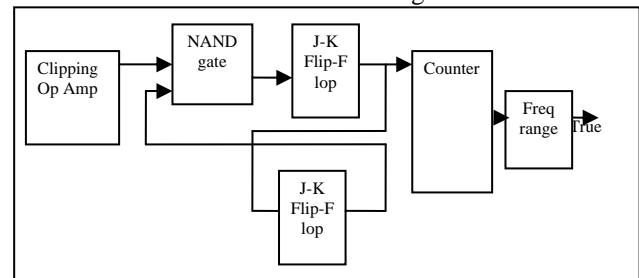
the band of 18 and 64 Hz as a false signal.

Fig.1 Block Diagram of the Ring Discriminator

A. Clipping Op-amp

A folded-cascode Op-Amp [2], [3] will be chosen as the topology of the clipping op-amp, so that its gain will be large enough to convert a sinusoidal signal into signal that similar to square-wave form. The concept of current mirror will be used in designing the op-amp. The Op-Amp is not used to amplify the incoming signal, its function is just to get a square waveform from the signal. In this work, the frequency for the signal is much more important. We can assume that the signal that have higher voltage level as HIGH logic level, while the signal that have lower voltage level as LOW logic level before connected to NAND gate. The higher voltage level is considered as 1.8 V and the lower voltage level is considered as < 0.04 V (lower than threshold voltage for a MOSFET to turn on). Fig. 2 shows the results of the clipping op-amp.
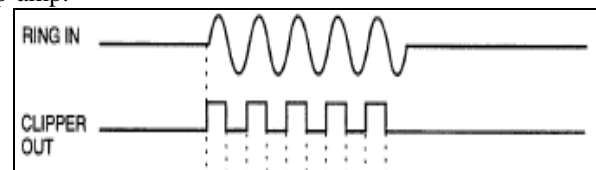

Fig.2 Output from Clipping Operational Amplifier

B. NAND Gates

The output from clipping operational amplifier and output from second flip-flop will be applied to the inputs of the NAND gate, so that NAND gate output will generate a clock for input CLK of J-K flip-flop (negative edge-triggered). The first flip-flop will only trigger when a HIGH to LOW signal. So, it will start to trigger at the end of one and a half of first ringing cycle.

C. Combination of J-K Flip-Flops

The purpose of these two flip-flops is to get an enable pulse for one cycle of ring sinusoidal signal. The output of NAND gate is applied to clock of first self-latching **J-K**

flip-flop. Initially all the flip-flops have to be cleared. The $\overline{Q}$ output of first flip-flop is connected to the clock input of a second self-latching J-K flip-flop, the output $\overline{Q}$ of second flip-flop is connected to the NAND gate as mentioned in previous section. It provides a LOW pulse with positive edge-triggering. This will set enable pulse at the Q output of first flip-flop.

The first J-K flip-flop will only toggle with negative edge-triggered, while the second J-K flip-flop will only toggle with positive edge-triggered. So, when the second flip-flop toggles at positive edge-triggered, a HIGH to LOW signal will be formed and is applied to the NAND gate. Then the output of NAND gate is applied to CLK of first flip-flop will have a HIGH logic level, will result the first flip-flop (toggle only negative edge-triggered) stop toggling to form an enable pulse at the output Q of flip-flop. This concept is shown in Fig. 3.
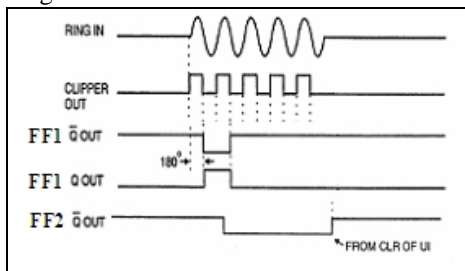

Fig.3 Enable pulse from NAND gate and Combination J-K flip-flops

D. Synchronous Binary Counter

The synchronous counter has an internal clock, and the external event is used to produce a pulse which is synchronized with this internal clock. This synchronous counter is enable by an enable pulse from output Q for the first latching flip-flop. A clock signal is also applied to the counter, preferably through an AND gate with the enable pulse. So, clock signal will only pass through AND gate to the counter during the interval of an enable pulse, which is enabled to count the clock pulses during that interval. The large numbers of bit are expected in this work, so the series carry synchronous counter are chosen [4] and [5].

E. Method to determine frequency range for incoming signal

Method to determine frequency range for incoming signal can be designed using one 2-input AND gates, one 2-input OR gates, one 2-inputs NAND gate. Fig. 4 explains the concept.
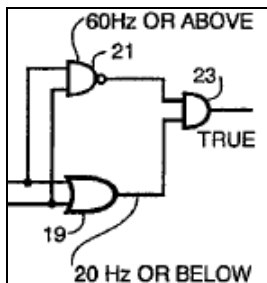

Fig.4 Logic gates to determine frequency range

III. RESULTS AND DISCUSSION

Results for the entire block will be discussed in this section with some figures, so that a better understanding can be gathered.

A. Clipping Op Amp

From Fig.5, we can found that the input transistors of the op-amp (input+ and input-) are ON when V_{GS} larger than 0.5915 V and it is amplified until it clip at 1.8 V. It is because the V_{dd} is 1.8 V. The output stage is limited to LOW level ($0 < V_{th}$) and HIGH level (1.8 V). This signal will act like a square waveform. This signal will later treated like a digital signal when applied to the NAND gate.
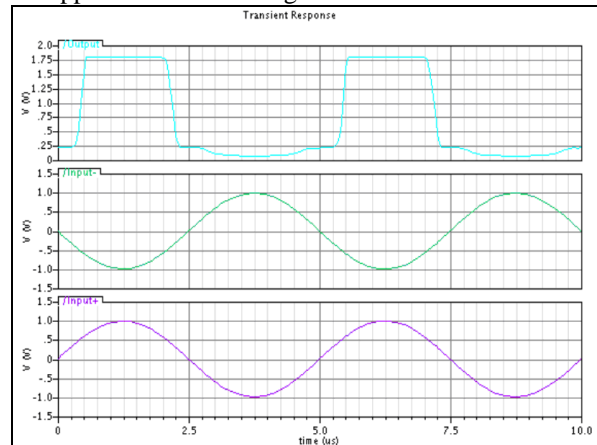

Fig.5 The transient response of Op-Amp
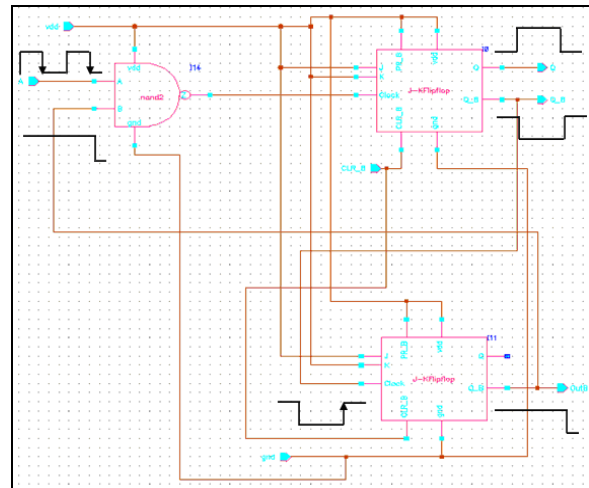
B. Combination of NAND gate and J-K flip-flop

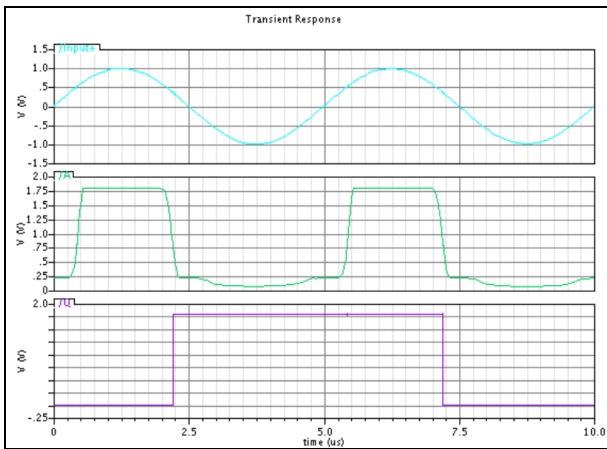Fig.6 Schematic of Combination two J-K flip-flops and NAND gate

Fig.7 Transient Response of Combination clipping Op-Amp and flip-flops

From Fig.6, the output of the clipping Op-Amp is applied to the input A of the combination flip-flops diagram. Since there is an NAND gate connected to the Clock of the first flip-flop, the first flip-flop will acts as negative-edge triggered with occurrence of inverter. Since all the flip-flops are initially cleared, then the *OutB* signal will be HIGH, complementary with the Q output of the second flip-flop.

As we can see from the schematic, the input A will be applied to the Clock of the first flip-flop with the feedback of the second flip-flop (*OutB*) using NAND gate. When there is a HIGH to LOW or negative-edge triggered Clock, the flip-flop will at the toggle state. It will toggle the Q output from LOW to HIGH and remain HIGH signal until the next negative-triggered Clock. The flip-flop will toggle the Q output again from HIGH to LOW. The flip-flop will continue to toggle at negative-edge triggered signal.

So, if there is no other condition that makes the first flip-flop stop toggling, then it will continue to toggle the output. That is the reason why we need another positive-edge triggering flip-flop and a NAND gate. The second flip-flop is a positive-edge triggered, and it will only toggle its output when there is a LOW to HIGH signal. So, the $\overline{Q}$ output of the first flip-flop has to apply to the Clock of the second flip-flop.

From the Q output of Fig.7, we can know that there is a LOW to HIGH signal at 7.2 μs for $\overline{Q}$ output. Initially, the second flip-flop is cleared, then it will toggle and have a LOW to HIGH at 7.2 μs for *Qut* Output. But giving a LOW to HIGH feedback signal will not stop the first flip-flop toggling. So, the *OutB* must be applied to apply to the NAND gate with a HIGH to LOW signal at 7.2 μs. When the LOW signal is applied to the NAND gate with the clipping Op-Amp, it will then clear the Op-Amp signal before it is applied to the Clock of the first flip-flop. Without the Clock edge triggered signal, then the flip-flop will stop toggling and generate an enable pulse with frequency of the incoming signal.

C. Synchronous Binary Counter

A synchronous Binary counter will be built using T flip-flop and a few AND gate. The logic diagram is shown as Fig.8.
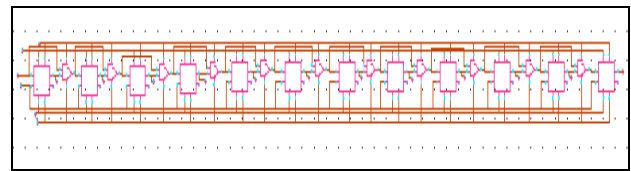

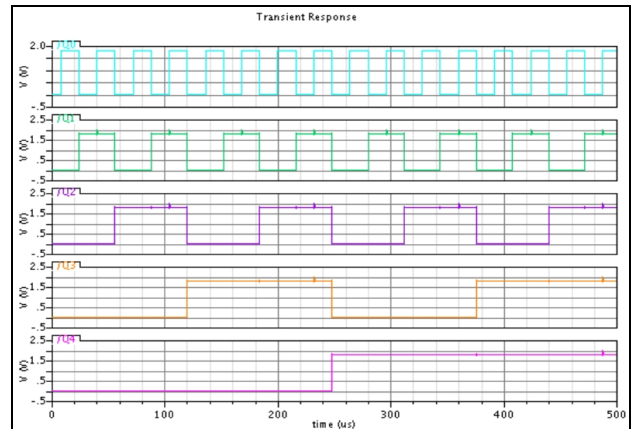Fig.8 Logic diagram of 12-bits Synchronous Counter with T flip-flop

Fig.9 Transient Response of Synchronous Counter (Q0 to Q4)

The period of the CLK for the counter is 16 us. Then the frequency, $f_{CLK} = 62.5$ kHz. As explain in the methodology that the frequency of the least significant bit (LSB), $f_{Q0} = 62.5 / 2 = 31.25$ kHz.

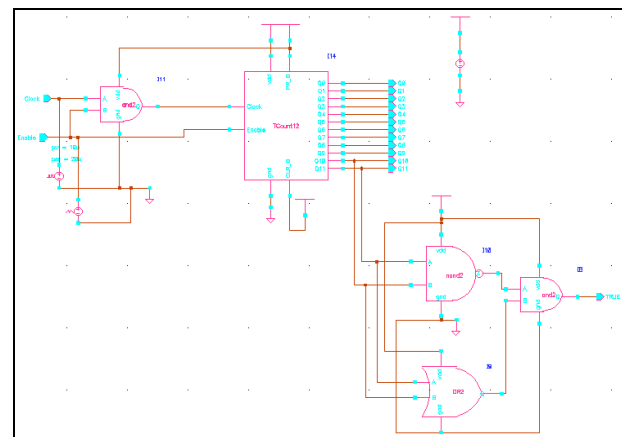*D. Method to determine frequency range for incoming signal*

Fig.10 Logic Diagram to determine frequency range

12 bits synchronous binary counter is created in the symbol form and most significant bit (MSB) Q11 and Q10 are connected with one NAND gate, one OR gate and one AND gate. With all of this logic gates, the frequency of the incoming signal can be determined whether it is within the range or not. Before the counter start counting, the Clock signal has to AND with the enable pulse and then is applied to the Clock of the counter. Besides that, the enable pulse also has to be applied to the Enable input to indicate when to start the counting.
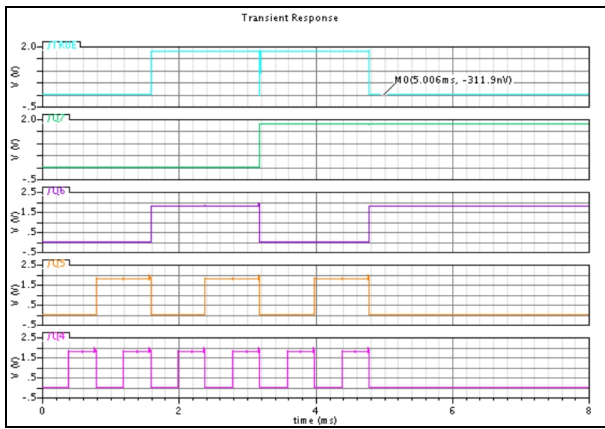
Fig.11 Counter with fCLK = 40 KHz and Enable pulse = 200 Hz

Fig.11 is a transient response of 8-bits synchronous counter and the frequency of the Clock is 40 kHz. The enable pulse will be set to 5 ms (200 Hz). Then when the logic gates that determine the frequency is connected to the MSB, Q7 and Q6, the TRUE signal shows that it will only turn on within the range from 1.6 ms to 4.8 ms (208 Hz to 625 Hz). Then when the enable pulse is 200 Hz < 208 Hz, the TRUE signal shows the LOW level at 5.006 ms means that the frequency of the incoming signal is below the range and it is an invalid signal.
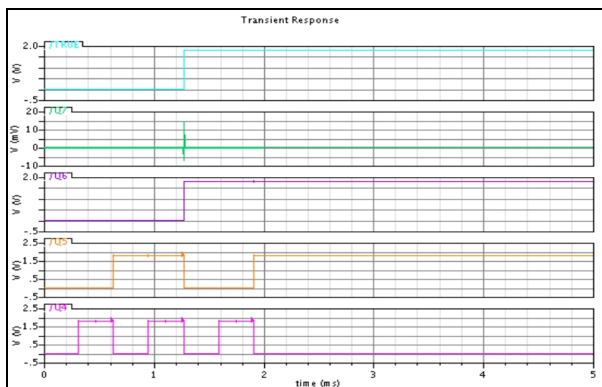

Fig.12 Counter with fCLK = 50 KHz and Enable pulse = 500 Hz

Fig.12 is a transient response of 12-bits synchronous counter and the frequency of the Clock is 50 kHz, means that the period of CLK is 20 us with different enable pulse which is 2.5 ms (500 Hz). From Fig.12, the TRUE signal shows that it will only turn on for the range of 1.28 ms to 3.84 ms (260.42 Hz to 781.25 Hz). So when the enable pulse is 260.42 Hz < 500 Hz < 781.25 Hz, the enable signal will cause the Q6 and Q7 stop counting and remain to the level before it stop counting. The TRUE signal shows that the HIGH level indicates the frequency of the incoming signal is within the range and it is a valid signal.

With different output bits from the output counter, we will get different frequency range. Besides that, different applied clock signal to counter will also cause different frequency rang e. Table 1 and 2 explain this issue.

TABLE 1 DIFFERENT FREQUENCY RANGE DETERMINED BY DIFFERENT INPUT BITS WITH fCLK = 50 KHZ

Inputs	Time	Frequency

		Min (ms)	Max (ms)	Min (Hz)	Max (Hz)
Q6	Q7	1.28	3.84	260.42	781.25
Q7	Q8	2.555	7.67	130.29	391.4
Q9	Q10	10.24	30.71	32.56	97.65
Q10	Q11	20.47	61.41	16.28	48.85

TABLE 2 DIFFERENT FREQUENCY RANGE DETERMINED BY DIFFERENT INPUT BITS WITH FCLK = 62.5 KHZ

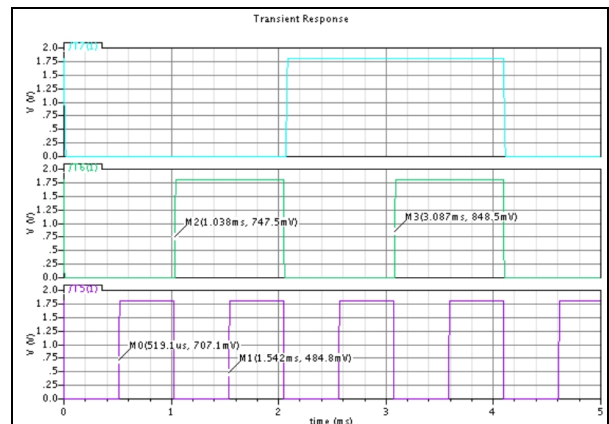| Inputs		Time		Frequency	
		Min (ms)	Max (ms)	Min (Hz)	Max (Hz)
T5	T6	0.5191	1.542	648.50	1926.40
T6	T7	1.038	3.087	323.94	963.39
T7	T8	2.025	6.172	162.02	493.83
T8	T9	4.122	12.35	80.97	242.60
T9	T10	8.306	24.69	40.50	120.39
T10	T11	16.62	49.35	20.26	60.17

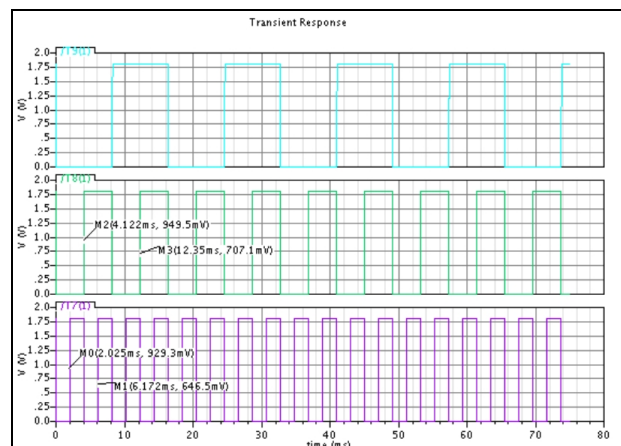Fig.13 Voltage for T5, T6 and T7 with its frequencies

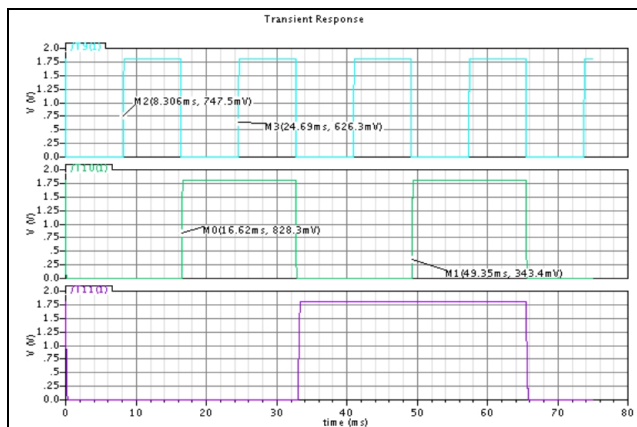Fig.14 Voltage for T7, T8 and T9 with its frequencies

Fig.15 Voltage for T9, T10 and T11 with its frequencies

From Table 2, we can know that their frequency range and there is a range that fulfill the requirement. They are the pair of T11 and T10. So, the frequency Clock of the counter has to be set to 62.5 KHz and connected the Q10 and Q11 to the NAND gate and OR gate according to the schematic (Fig. 10). Fig. 13, 14 and 15 show the signal of the counter outputs.

IV. CONCLUSION

The frequency discriminator which is designed for the ringer has proved to be working. The frequency of the incoming ring signal can be determined whether it is within frequency band or not. The frequency range that assumed as a valid signal for this work is within 20 Hz to 60 Hz. So in this work, the Clock signal for the counter has been adjusted to 8 μs to get more precise frequency range for the ringer integrated circuit. As a conclusion for this work, the most important parameter that has to be considered is the frequency.

REFERENCE

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