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FPGA Implementation of Multilevel Space Vector PWM Algorithms

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***Abstract* – Multilevel converters can meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interface. With the increase in number of levels, it is necessary to control more and more switches in parallel. Field programmable gate arrays (FPGAs), with their concurrent processing capability, are suitable for the implementation of multilevel modulation algorithms. Among them, space vector pulse width modulation algorithms offer great flexibility to optimise switching waveforms. In this paper the SVPWM technique is analysed and implemented in FPGA. The SVPWM pulses thus generated through the FPGA tool is given as switching pulses to the VSI circuit to trigger the three phase induction motor. FPGA is chosen due to its fast prototyping, simple hardware and software design. Simulation results are provided along with the theoretical analysis in terms of THD, output fundamental voltage and voltage transfer ratio to verify the feasibility of operation.**

***Index Terms* - Field programmable gate array (FPGA), voltage source inverter (VSI), space vector pulse width modulation (SVPWM), Printed circuit board (PCB).**

I. INTRODUCTION

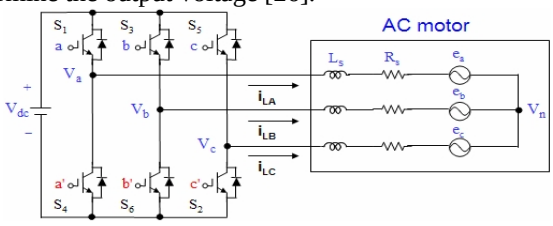
PWM inverters are becoming more and more popular in today's motor drives. Sinusoidal Pulse Width Modulation (SPWM), is used to control the inverter output voltage and maintains a good performance of the drive in the entire range of operation between zero and 78 percentage of the value that would be reached by square operation [1][2]. The Pulse Width Modulation (PWM) Technique called "Vector Modulation", which is based on space vector theory, is the most important development in the last few years[3][4][5]. Although, several of PWM methods have been created in the past, the vector modulation technique appears to be the best alternative for a three phase switching power converter [6][7][8]. FPGA's development reached a level of maturity that made them the choice of implementation in many fields[9].Recent applications of FPGA's in industrial electronics include mobile- robot path planning and intelligent transporation [10][11],current control applied to power converters [12][13],real-time hardware in the loop testing for control design[14], controller implementation [15][16], separating and recovering independent source signals[17], and neural computation[18]. Since the concept of multilevel PWM converter was introduced, various modulation strategies have been developed and studied in detail, such as multilevel sinusoidal PWM, multilevel selective harmonic elimination and space vector modulation. Among these strategies, the space vector PWM (SVPWM) [19][20] stands out because it offers significant flexibility to optimize switching waveforms and is well suited for digital implementation. Complexity and computational cost of traditional SVPWM techniques increases with the number of levels of the converter, and most of all use trigonometric functions or precomputed tables [21][22].The implementation of FPGA of in SVPWM control for a voltage source inverter has been described in detail in [23][24]

A symmetrical space vector modulation PWM pattern is proposed in this paper, it shows the advantage of lower THD without increasing the switching losses. Thus this paper demonstrates that a more efficient and faster solution is the use of Field Programmable Gate Array (FPGA's),it investigates how to generate a variable PWM waveform based on Xilinx FPGA [25]and the proposed design is tested by functional/timing simulation and experiments.

The rest of the paper is organized as follows. Section II briefly introduces the principle of symmetrical space vector PWM method. Section III details on FPGA. Section IV the hardware circuit which acts as the interface between the FPGA and the VSI circuit. Section V explains the experimental results and Section VI is the conclusion

II. PRINCIPLE OF SPACE VECTOR PWM

The circuit model of a typical three-phase voltage source PWM inverter is shown in Figure 1 S1 to S6 are the six power switches that shape the output, which are controlled by the switching variables a, a', b, b' and c, c'. When an upper transistor is switched on, i.e., when a, b or c is 1, the corresponding lower transistor is switched off, i.e., the corresponding a′, b′ or c′ is 0. Therefore, the on and off states of the upper transistors S1, S3 and S5 can be used to determine the output voltage [26].

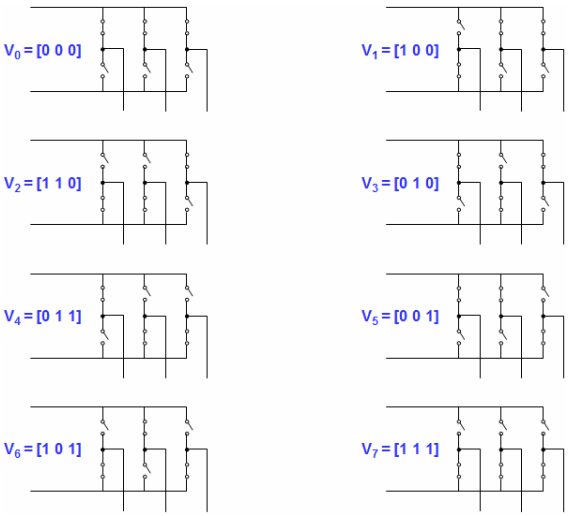


There are eight possible combinations of on and off patterns for the three upper power switches. The on and off states of the lower power devices are opposite to the upper one and so are easily determined once the states of the upper power transistors are determined. According to equations and,

the eight switching vectors, output line to neutral voltage (phase voltage), and output line-to-line voltages[26] in terms of DC-link Vdc, are given in the Table 1 [27] and Figure 2 shows the eight inverter voltage vectors[28] (V0 to V7).

Table 1. Switching vectors, phase voltages and output line to line voltage

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0



Space Vector PWM (SVPWM) refers to a special switching sequence of the upper three power transistors of a three-phase power inverter. It has been shown to generate less harmonic distortion in the output voltages and currents applied to the phases of an AC motor and to provide more efficient use of supply voltage compared with sinusoidal modulation technique as shown in Figure 5 [28]

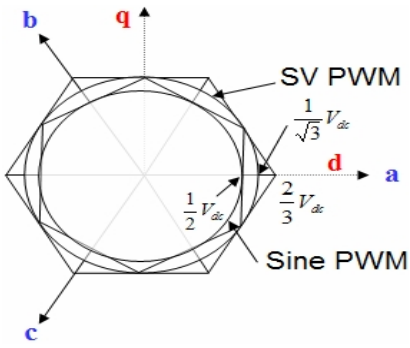


Fig 3: Locus comparison of maximum linear control voltage in Sine PWM and SVPWM.

To implement the space vector PWM, the voltage equations in the abc reference frame can be transformed into the stationary dq reference frame that consists of the horizontal (d) and vertical (q) axes as depicted in Figure 4 [28]

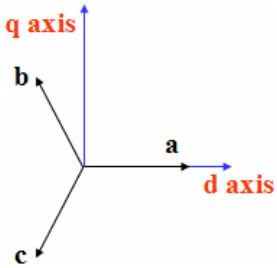


Fig 4: The relationship of abc reference frame and stationary dq reference frame.

As described in Figure, this transformation is equivalent to an orthogonal projection of [a, b, c]t onto the two-dimensional perpendicular to the vector [1, 1, 1]t (the equivalent d-q plane) in a three-dimensional coordinate system[29]. As a result, six non-zero vectors and two zero vectors are possible. Six nonzero vectors (V1 - V6) shape the axes of a hexagonal as depicted in Figure 5 and feed electric power to the load. The angle between any adjacent two non-zero vectors is 60 degrees. Meanwhile, two zero vectors (V0 and V7) are at the origin and apply zero voltage to the load. The eight vectors are called the basic space vectors and are denoted by V0, V1, V2, V3, V4, V5, V6, and V7. The same transformation can be applied to the desired output voltage to get the desired reference voltage vector Vref in the d-q plane. The objective of space vector PWM technique is to approximate the reference voltage vector Vref using the eight switching patterns. One simple method of approximation is to generate the average output of the inverter in a small period, T to be the same as that of Vref in the same period[26].The only difficulty in this method is the trigonometric calculations[29].

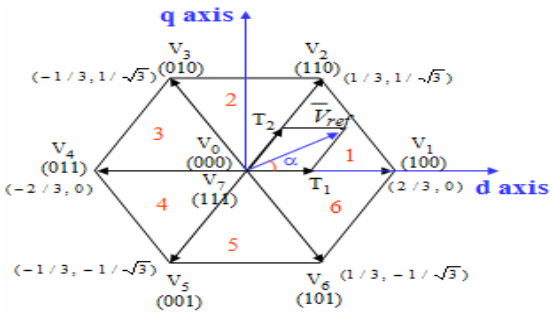


Fig 5. Basic switching vectors and sectors

Therefore, space vector PWM can be implemented by the following steps:

Step 1. Determine Vd, Vq, Vref, and angle (α)
Step 2. Determine time duration T1, T2, T0.
Step 3. Determine the switching time of each transistor (S1 to S6).

III. FIELD PROGRAMMABLE GATE ARRAY

A Field-Programmable Gate Array or FPGA is a silicon chip containing an array of configurable logic blocks (CLBs). Unlike an Application Specific Integrated Circuit (ASIC)

which can perform a single specific function for the lifetime of the chip an FPGA can be reprogrammed to perform different function in a matter of microseconds. The design used Xilinx development tools, namely Workview, and is realized in a single FPGA chip with no external memory. The benefits of this design are as follows [30][31]

The whole system is implemented in only a single chip consequently the circuit is very compact.
Systems of FPGA chip are more reliable because they do not need any control software.
Faster design and verification time, design change without penalty.

In this paper programming FPGA using Hardware Description Languages and coding are used to generate the Space Vector Modulation for the inverter circuit. The Hardware Description Language is familiar to the vast number of software programmers and since VHDL is very much common to most of the programmers it becomes easier for individuals to work in this software.

A very attractive high-level design/simulation tool is provided by FPGA and is called XILINX. It is a very flexible design tool, which allows Testing of a high-level structural description of the design and makes possible quick changes and corrections. The circuit description structure is very similar to the way the design could be implemented later. Therefore mapping tool allowing conversion of such a structure into VHDL code would save the designer's time, which otherwise has to be spent in rewriting the same structure in VHDL and probably making mistakes that will need debugging.

Simulation Steps:
1). Initialize system parameters using FPGA
2). Perform VHDL coding to
Determine sector
Determine time duration T1, T2, T0
Determine the switching time (Ta, Tb, and Tc) of each transistor (S1 to S6)
Generate the inverter output voltages (ViAB, ViBC, ViCA,) for control input (u)
Burn the program in the FPGA kit
3) View the SVPWM waveforms through xilings

IV. HARDWARE IMPLEMENTATION

Power MOSFETs, with their insulated gates, are voltage driven. A basic knowledge of the principles of driving the gates of these devices will allow the designer to speed up or slow down the switching speeds according to the requirements of the application. It is often helpful to consider the gate as a simple capacitor when discussing drive circuits.

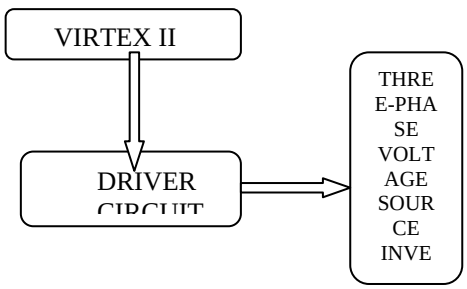


Fig 6. Overall Block Diagram

The coding is written using VHDL and is dumped in the Virtex kit. Doing this the FPGA kit will function according to the instruction given through the coding. Here, the FPGA will generate six PWM signals in case of 1s and 0s. This signal is given as input to the driver circuit which will almost amplify the 3.3 V input supply up to 12 volt, which is enough for triggering the gate terminal of the MOSFET.

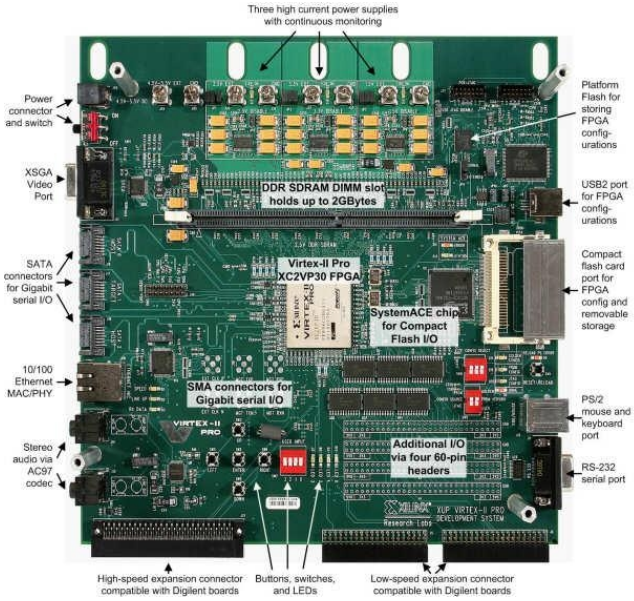
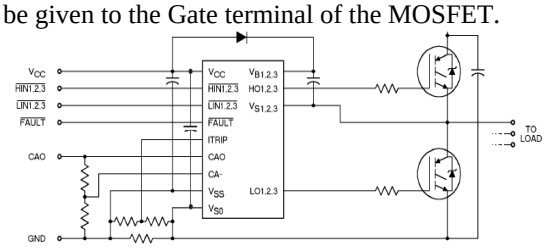


Fig 7. Xilinx Virtex IIP

Virtex and Spartan are the two FPGA family kits manufactured by Xilinx. Virtex is an advanced version than the Spartan and hence its cost is also much more compared to Spartan.Here Virtex II Pro- XC2VP30 is used which supports Xilinx 9.2 version for programming. The power supply given to the kit is of 5 V, and a voltage of 3.3V and 1.8 V can be obtained.

DRIVER CIRCUIT

Voltage level is amplified after receiving pulses from optocoupler. Current level is amplified using coupled transistor. To turn ON the transistors OR for biasing 12V the transformer is used. It is converted into DC using a bridge rectifier. The amplified pulse is taken as output from the Emitter of the coupled transistor. The amplified output pulse will be given to the Gate terminal of the MOSFET.



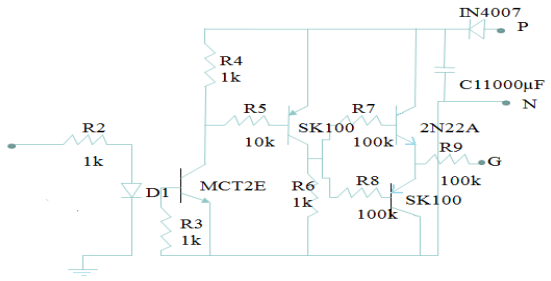


Fig 8.Driver circuit

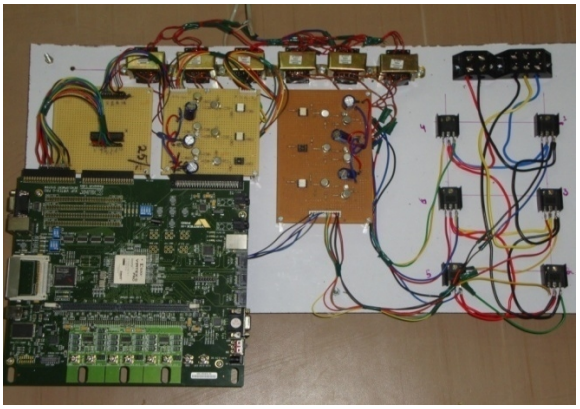


Fig 9.Hardware Model

V. SIMULATION RESULT

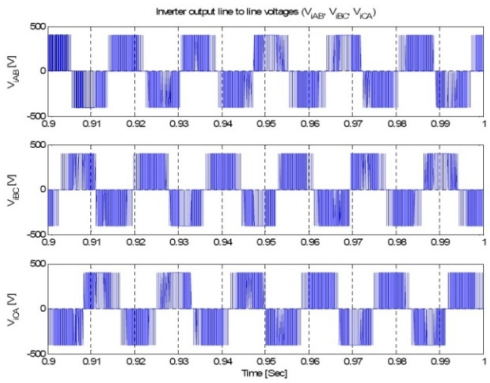


Fig 10. Simulation results of inverter output line to line voltages

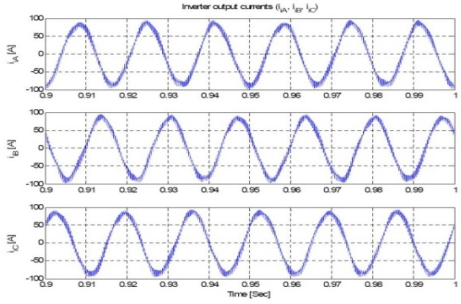
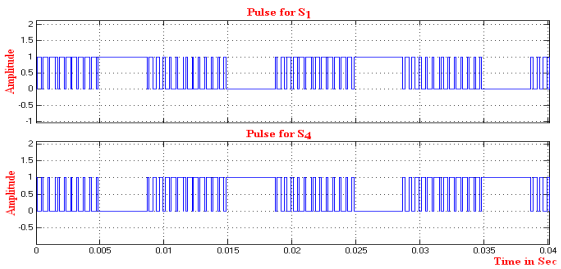


Fig 11. Simulation results of inverter output currents



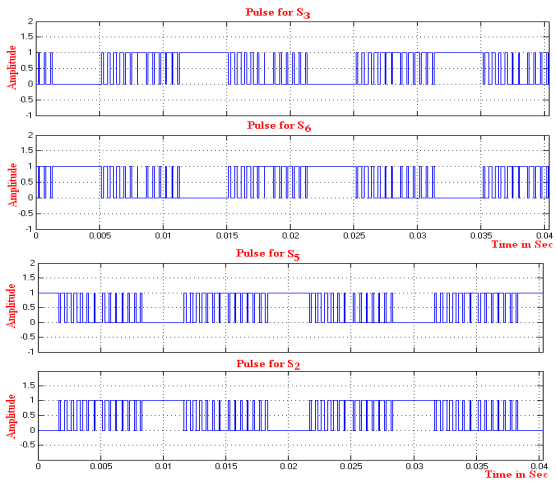


Fig 12. Triggering SVPWM pulses for the VSI circuit

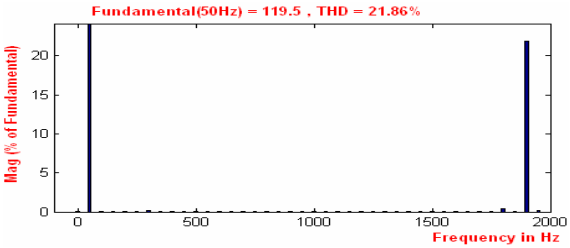


Fig 13. FFT Analysis of Output Voltage (SVPWM)

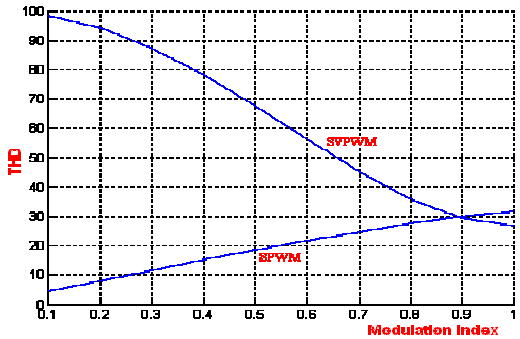


Fig 14. Fundamental & THD Vs Modulation Index (m)

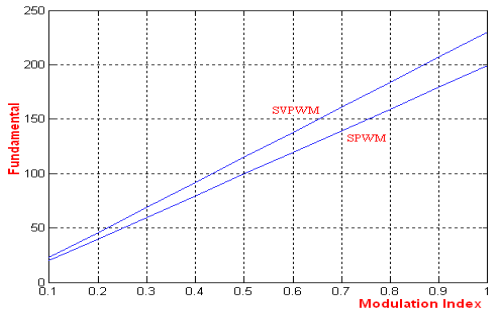


Fig 15.Fundamental Voltage Comparison of SVPWM & SPWM

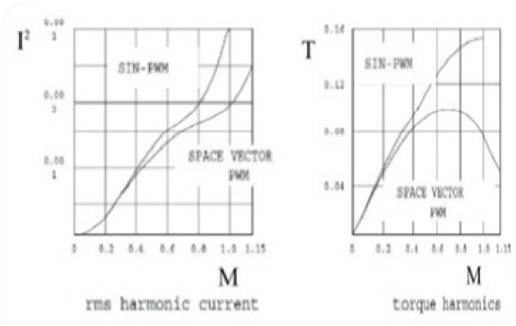


Fig 16. Harmonic Comparison of SVPWM & SPWM

Voltage Utilization: SPWM: Vmax= Vdc/2 ;
SVPWM: Vmax=Vdc/sqrt(3)
Space Vector PWM = 2/√3 times of S

VI. CONCLUSION

In this paper, a theoretical study concerning the SVPWM control strategy on the voltage inverter based on FPGA is presented. This aims on the one hand to prove the effectiveness of the SVPWM in the contribution in the switching power losses reduction. SVPWM is among the best solution to achieve good voltage transfer and reduced harmonic distortion in the output of an inverter.

Since Field programmable gate array (FPGA) have better advantages compared to microprocessor and DSP control, this modulation technique is implemented in an FPGA. The FPGA coding makes it easier in designing the vector modulation pattern generator using field programmable Array.

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