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The Analysis of Parameter Limitation in Diode-Clamped Resonant Gate Drive Circuit

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***Abstract*—Switching loss has to be reduced in order to improve converter's performance and efficiency. In high switching frequency, the effect of the loss is much greater. The duty ratio, dead time and inductor value are the limiting parameters which bring implications on the switching loss and hence total gate drive loss. Using PSpice circuit simulator, the optimization of these parameters have been carried out and it is found that the duty ratio, dead time and resonant inductor value are 20 %, 15 ns and 9 nH respectively. The details for choosing these values are presented in this paper.**

***Index Terms*—PSpice simulation; resonant gate drive; switching loss**

I. Introduction

IN megahertz frequency converter design, resonant gate drive (RGD) circuit network is normally chosen due to its ability in resulting lower power loss, high efficiency and speed. The effect of RGD on overall performance of converter becomes more critical as frequency increases. Thus, there have been many RGD circuit introduced in the recent years to look for solutions in loss reduction, where most of them employed LC resonance configuration techniques [1-11]. At very high frequency (VHF), the effect of gate drive circuit on overall performance and efficiency of converter becomes critical. Further increase in frequency may cause power density to degrade, increase gate driving loss [12] and eventually this gives rise to many limitations in the converter circuit design when employing high power switching devices. Some reviews on high frequency converter design are summarized in [13].

This paper is dedicated to analyze and optimize the power losses in the RGD circuit particularly in the diode-clamped configuration. In recent years, diode-clamped RGD circuit has been introduced and it is claimed to have full capability in recovering energy without high dissipation at the input source [14]. However, there are limitations in the RGD where the resonant inductor value used must adhere to certain factors. The implications of duty ratio, D, dead time, T_D and resonant inductor, L_r are essential in achieving high frequency gate drive operation. Design of these parameters may influence the switching losses in the circuit. In this work, a discrete high power MOSFET is chosen as a switch because it could operate up to 5 MHz [15].

There are several types of losses in the RGD circuit such as conduction loss, gate drive loss and switching loss. Switching loss is the main contributor. Higher switching loss indicates higher heat dissipation, and hence may lead to circuit malfunction. Fig. 1 shows the diode-clamped RGD circuit where VP_1 and VP_2 are two separate pulse generators which provide complementary square wave periodic signals to both switch Q_1 and Q_2 respectively. The pulsating wave oscillates at 1 MHz switching frequency.

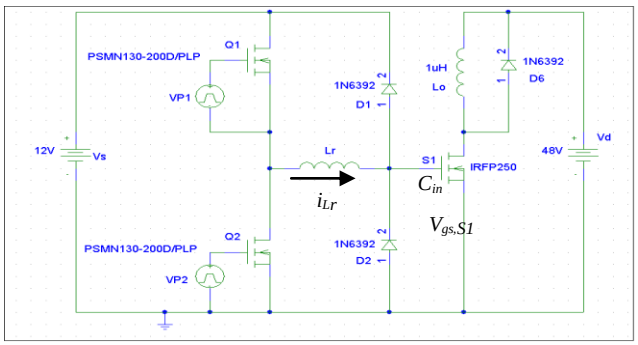

Fig 1. Diode- clamped RGD circuit

By getting the pulses from VP_1 and VP_2, Q_1 and Q_2 will produce waveforms as shown in Fig. 2. When Q_1 is turned on, the inductor current, i_{Lr} starts to develop. Switch Q_2 at this time is not conducting. Here, i_{Lr} is charged to maximum value and so is $V_{gs,S1}$. This $V_{gs,S1}$ increases exponentially and then is clamped to input source, V_s of 12 V. The duration of the charging current depends on L_r and the impedance, Z_0 being the time constant of the circuit. Once it is fully charged, i_{Lr} starts to discharge to zero through body diode of Q_2, L_r, D_1 and back to V_s. For a specified time given after Q_1 is turned off, Q_2 takes its turn to conduct. This specified time s known as dead time, T_D. Then the previously clamped 12-$V_{gs,S1}$ is discharged to zero.

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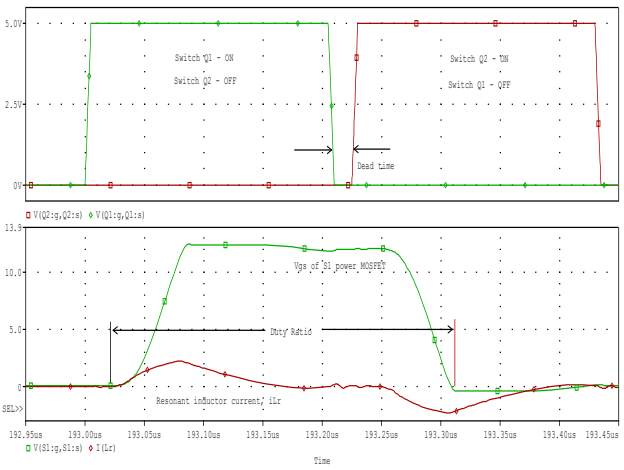

Fig. 2. Operating waveforms of diode-clamped RGD circuit

The i_{Lr} is charged again to maximum but now in the negative direction. Once charged, it is charged back to zero [16-17]. In the simulation, the driving switches Q_1 and Q_2 are of Phillips PSMN130-200D (200 V/20 A), a power MOSFET, S_1 from Fairchild Semiconductor IRFP250 (200 V/33 A) and two fast recovery diodes manufactured by International Rectifier 1N6392 (45 V/60 A).

II. Limitations & Implications On Diode-Clamped RGD Circuit

Discussion about limitations in the RGD circuit design and their implications are very limited. The variation in pulses of VP_1 and VP_2 can influence the operating duty ratio, D. Duty ratio determines the length of conduction time of power MOSFET, S_1 and it has to have sufficient ON time for i_{Lr} to completely charge and discharge. As inductor L_r increases, the longer i_{Lr} takes to conduct. This results in oscillation during turn-off and eventually generates higher switching loss. Also, by varying T_D, the consequences may both add to the further switching loss and speed reduction. This in turn necessitates optimizing D, T_D and L_r in the tradeoff between size of L_r, switching loss and speed of diode-clamped RGD circuit.

PSpice circuit simulator is used to investigate these limiting factors and their implications in the RGD circuit design. Using the predesigned diode-clamped RGD circuit [16], the D, L_r and T_D are varied in order to obtain an optimized switching loss in the circuit. By maintaining a constant load, the effects of varying parameter values on the implications of the switching loss are observed. The conclusions are then drawn from this.

A. Effects of Duty Ratio, D

The summation of charging and discharging time of i_{Lr} is used as a benchmark in determining the minimum range of D. As shown in Fig. 3, the 200 ns pulse width out of 1 MHz switching frequency indicates a portion of 20 % turn-on from one cycle. Here, during the conduction of Q_1, i_{Lr} is charged to maximum. Then the discharging phase will commence only when i_{Lr} is fully charged until it reaches back to zero.

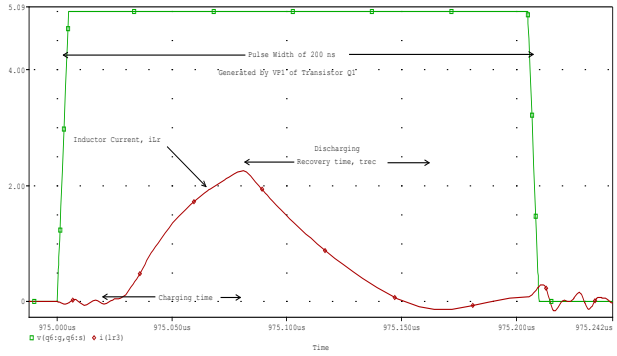

Fig. 3. Charging & discharging i_{Lr} with respect to duty ratio, D

The discharged current of i_{Lr} also requires a considerable amount of time before the turn-on sequence ends. This is known as the recovery time, t_{rec} (1) where C_{in} is the input capacitance of power MOSFET, S_1 and its duration is normally longer than the charging time.

$$t_{rec} = \sqrt{L_r C_{in}} \tag{1}$$

The duration of charging is shorter due to ON resistive charging effects through gate and driver resistance. A faster recovery diode can be used to improve faster charging time and thus speed of the converter. VP_1 has to provide sufficient ON-time which will allow i_{Lr} to flow without disruption. In the next sequence when Q_2 conducts, Q_1 is off.

The i_{Lr} charging and discharging behavior of Q_2 are identical to Q_1. However, the negative peak i_{Lr} of Q_2 is slightly reduced. This is due to higher parasitic resistance gained in S_1's C_{in} during the switching transition. Increasing pulse width in VP_1 and VP_2 will increase D of $V_{gs,S1}$. On the other hand, reducing the pulse width too narrow may force discharged i_{Lr} to oscillate at the end of turn-off transient in $V_{gs,S1}$. This consequently increases dissipation and gives rise to stress in the diode-clamped RGD circuit.

B. Effects of L_r

In the resonant network, i_{Lr} charges and discharges with respect to the applied pulse width of VP_1 and VP_2. Thus, the gate terminals of Q_1 and Q_2 will draw current for a short duration of time which is used to fully charge the $V_{gs,S1}$. Here, i_{Lr} is at maximum. The time taken for i_{Lr} to reach maximum from zero is called the rise time, t_{rise} (2).

$$t_{rise} = \frac{\pi}{2}\sqrt{L_r C_{in}} \tag{2}$$

As L_r value increases, the charging and discharging time of i_{Lr} also increase. From Fig. 4, there shows a limit in L_r for the generation of $V_{gs,S1}$ before i_{Lr} starts to oscillate at turn-off. Using 200 ns pulse width, L_r of 40 nH or below is chosen for T_D of 15 ns. It is anticipated that when higher L_r is used, i_{Lr} will produce ringing and thus increase diode conduction loss.

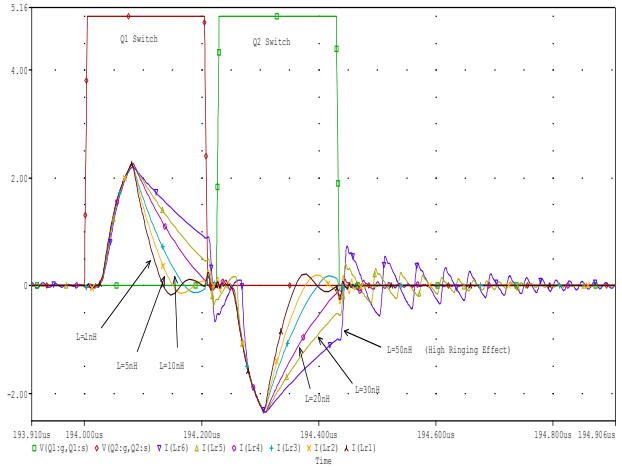

Fig. 4. Varying i_{Lr} for 200 ns pulse width at T_D of 15 ns

During the conduction of either Q_1 or Q_2, i_{Lr} increases exponentially to maximum either positive or negative peak value before discharging. The i_{Lr} equation is given in (3) where R_g is the total gate resistance in the diode-clamped RGD and this value is approximately between 1.3 Ω and 1.7 Ω. The time taken for i_{Lr} to reach peak value is given in (4). The shorter the time, the faster the turn-on speed will be. The $V_{gs,S1}$ is dependent on C_{in} and the integral of i_{Lr} as given in (5).

$$i_{Lr}(t) = \frac{2V_s}{\sqrt{\frac{4L_r}{C_{in}} - R_g{}^2}} e^{-\frac{R_g}{2L_r}t} \sin\left(\frac{\sqrt{\frac{4L_r}{C_{in}} - R_g{}^2}}{2L_r}t\right) \quad (3)$$

$$tpeak = \frac{\tan^{-1}\left(\frac{2L_r\sqrt{\frac{4L_r}{C_{in}} - R_g{}^2}}{R_g}\right)}{2\sqrt{\frac{4L_r}{C_{in}} - R_g{}^2}} \quad (4)$$

$$V_{gs,S1}(t) = \int_0^t \frac{1}{C_{in}} i_{Lr}(t)dt \quad (5)$$

During turn-on, the charging time of i_{Lr} will represent the turn-on speed of the circuit as mentioned in (1). Increasing L_r will result in increasing turn-on time and hence leading to a slower speed. However, introducing a very small L_r will reduce the transient response at the cost of limiting the operating current flow within the resonant tank. This eventually increases peak current of i_{Lr} and consequently produces higher power loss.

So, L_r has to be optimized in the tradeoffs between speed and switching losses. Switching loss is directly proportional to speed. In order to reduce switching loss, one option is to reduce the speed. However, this is not desirable in high frequency application. T_D is also important in the optimization of switching losses. Having an optimized T_D value between Q_1 and Q_2 conduction cycles, this can prevent shoot-through or cross conduction of signals and hence reduce the loss. Fig. 5 shows the relationship between L_r and peak current of i_{Lr} for different T_D values ranging from 1 ns to 30 ns. For all T_Ds, it is found that the optimized value of L_r is found to be around 9 nH.

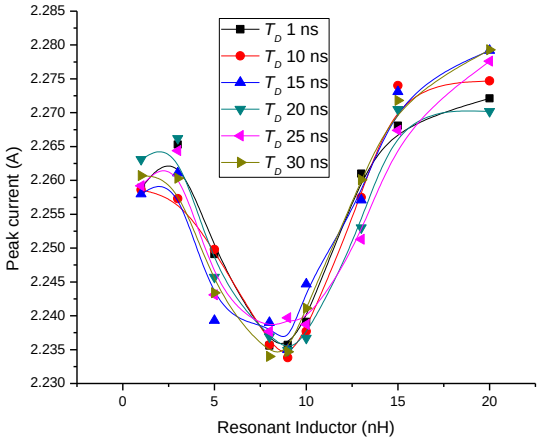

Fig. 5. Graph of peak current vs L_r for different T_D values

C. *Effects of T_D*

A fixed dead time control technique is used due to its simplicity. T_D can be easily set up to avoid shoot through or cross conduction between gates of Q_1 and Q_2 as they are conducting complementarily. Using the optimized L_r of 9 nH, the i_{Lr} of different T_D values during turn-off phase are observed via simulation.

As shown in Fig. 6, it is found that there are presence of ringing in i_{Lr} which may cause variation in power losses at $V_{gs,S1}$ at turn-off. It is also observed that when T_D is set small, there are more ringing counts. On contrary, increasing T_D can reduce this effect. However, if T_D is applied too long, $V_{gs,S1}$ will appear floating and hence this may give further rise to higher dissipation in the circuit.

In addition, the T_D value can be determined from the tradeoff between speed and high power dissipation at turn-off. Referring to Fig. 7, longer T_D introduces higher ringing overshoot voltage. This pattern comes from the energy stored in the parasitic inductance when it is released across parasitic capacitance of S_1. Thus, based on the design parameters, it is found that the optimized T_D value is 15 nH, as shown in Fig. 8.

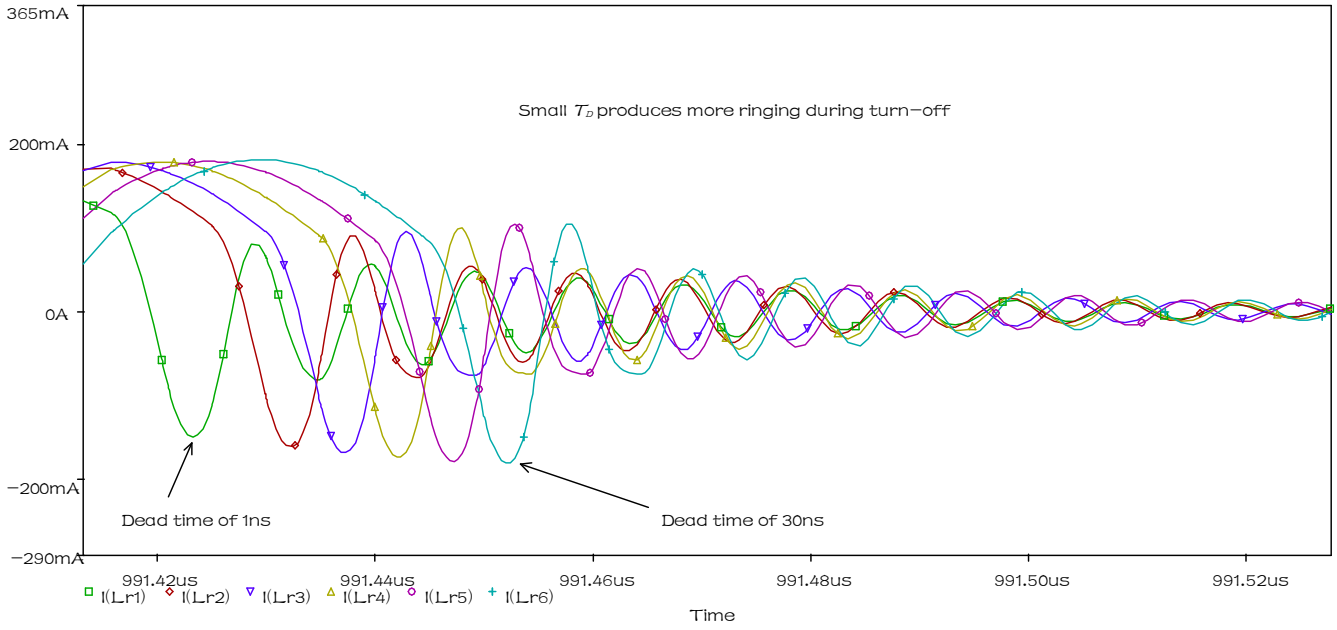

Fig. 6. Ringing effect in i_{Lr} at turn-off for different T_D with L_r of 9 nH

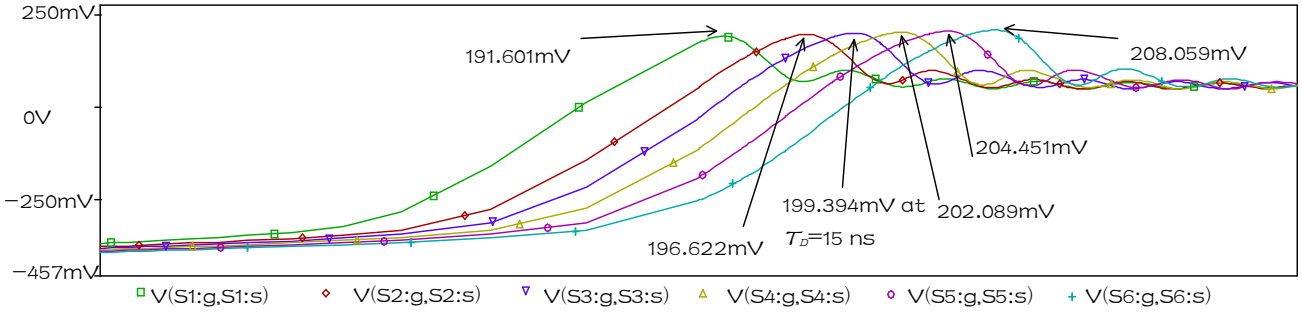

Fig. 7. Ringing effect in $V_{gs,S1}$ at turn-off for different T_D with L_r of 9 nH

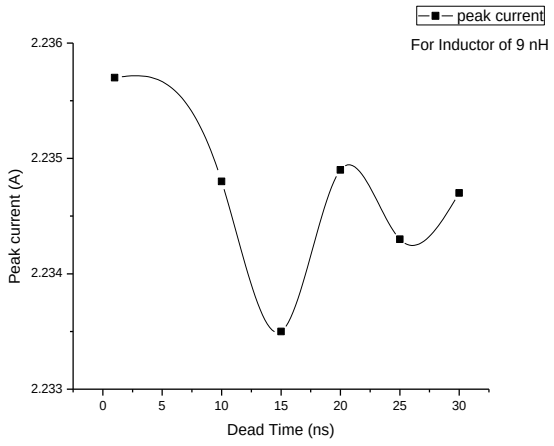

Fig. 8. Optimized T_D value at lowest peak current of i_{Lr}

III. Results & Discussions

In diode-clamped RGD circuit, the charging and discharging of i_{Lr} generates a resonant link between S_1 and V_s. Comparing to the conventional totem-poled gate drive circuit, more energy could be saved. Generally, the switching loss in RGD circuit is high especially in the driving transistors Q_1 and Q_2. This loss is usually caused by rapid switching transition of ON and OFF in the transistors. Where switching loss is a variable parameter that consistently changes with respect to variation in L_r, T_D and D, this can be reduced by adopting snubber network [18-20].

By lowering the peak current of i_{Lr}, this will lead to a faster turn-on speed. In this case, different L_r and fixed t_{rise} are applied, giving different peak current values. Consequently, the efficiency of the diode-clamped RGD circuit can be improved significantly. The power loss equations for driving switches Q_1-Q_2, diodes D_1-D_2 and gate voltage S_1 are given in (6-8) respectively.

$$P_{sw} = V_{ds} * i_{ds} \tag{6}$$

$$P_{diode} = \frac{2V_f}{2V_f + V_s} * \frac{\sqrt{\frac{Lr}{Cin}}}{Rg + \sqrt{\frac{Lr}{Cin}}} Q * V_s * f_s \tag{7}$$

$$P_{gate,\,S1} = i_{Lr} * V_{gs,\,S1} \tag{8}$$

where V_f is forward voltage drop of D_1 and D_2, Q is the gate

charge of S_1 and f_s is the switching frequency. From simulation, the switching loss of Q_1 and Q_2 are dominant. By applying higher L_r, this results in lower peak current and thus reduces switching loss.

Nevertheless, there will be an upper limit of L_r where increasing it too high will force i_{Lr} to generate high oscillation in the circuit. The switching loss in D_1 and D_2 is minimal. The $V_{gs,S1}$ power loss is about one half (222 mW) of the switching loss in Q_1 (418.02 mW) and Q_2 (453.47 mW).

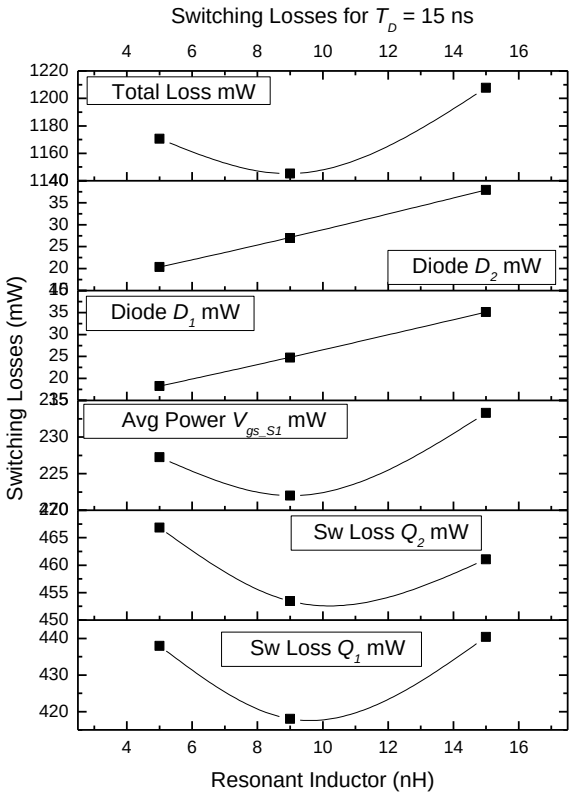

Fig. 9 Switching loss distribution in diode-clamped RGD circuit

Fig. 9 shows the distribution of switching loss in the diode-clamped RGD circuit. It is noticeable that the switching loss in transistors is high and dominant. Further studies on the application of snubber circuits are highly recommended. Both switching loss in diodes behave linearly as L_r increases because more time required for i_{Lr} to charge and discharge within the circuit and along the diode path. This adds to the oscillation of i_{Lr} which contributes to the loss.

The average gate voltage of S_1 is found to be 222 mW, which makes up of 19.4 % out of total switching loss of 1145 mW at 9 nH with T_D of 15 ns, D of 20 % and f_s of 1 MHz. If the switching loss of Q_1 and Q_2 can be further reduced, this will eventually reduce more loss in S_1. The diode-clamped RGD circuit will definitely be able to operate in higher switching frequency, together will proper T_D control and thus reduce the stress of S_1 and operate with better efficiency.

IV. Conclusions

In the design of diode-clamped RGD circuit, reducing switching loss is vital. In megahertz frequency, the converter's performance and efficiency can easily be affected by high switching loss in the circuit. This paper discusses about the limiting parameters such as duty ratio, dead time and choice of inductor value which requires optimization and how these can bring implications on the switching loss in the circuit. Using PSpice circuit simulator, the optimization technique has been carried out and from the analyses, it is found that the duty ratio, dead time and resonant inductor are 20 %, 15 ns and 9 nH respectively. Consequently, the converter can optimize the total switching loss in the circuit and operate more efficiently in high frequency environment.

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References

[1] H. Wang and F. Wang "A Self-powered resonant gate driver for high power mosfet modules" *IEEE Applied Power Electronics Conference and Exposition*, pp. 183-188, 2006.

[2] T. Lopez, G. Sauerleander, T. Duerbaum and T. Tolle "A detailed analysis of resonant gate driver for PWM applications" *IEEE Applied Power Electronics Conference and Exposition*, Vol. 2, pp. 873-878, Feb. 2003.

[3] D. Sobczynski "Active gate drivers" *28th International Spring Seminar*, pp. 236-239, 2005.

[4] Y.H. Chen, F.C. Lee, L. Amoroso and H. Wu "A resonant MOSFET gate driver with energy efficient recovery" *IEEE Transactions on Power Electronics*, Vol. 19, No. 2, pp. 470-477, Mar. 2004.

[5] L. Balogh "Design and application guide for high speed MOSFET gate drive circuits" *Texas Instrument Application Notes*, pp. 1-37, Sep. 2007.

[6] Y.H. Chen, F.C. Lee, L. Amoroso and H. Wu "A resonant MOSFET gate driver with complete energy recovery" *IEEE Power Electronics and Motion Control Conference*, Vol. 1, pp. 402-406, 2000.

[7] K. Yao and F.C. Lee "Novel resonant gate driver for high frequency synchronous buck converters" *IEEE Transactions on Power Electronics*, Vol. 17, No. 2, pp. 180-186, Mar. 2002.

[8] I. Omura and Y. Shi "Gate driving circuit and gate driving method of power MOSFET" *U.S. Patent Application Publication*, pp. 1-9, Feb. 2006.

[9] B.S. Jacobson "High frequency resonant gate driver with partial energy recovery" *Power Electronics Specialists Conference*, pp. 131-141, 2001.

[10] N.Z. Yahaya "Improvement of high-power and high-frequency GaN HEMT converter" *5th UTP Postgraduate Symposium*, Jul. 2007, unpublished.

[11] N.Z. Yahaya, K.M. Begam and M. Awan "Simulation of an inductive coupled high frequency resonant gate driver circuit" *IEEE Industrial Informatics*, pp. 1523-1527, Jul. 2008.

[12] W. Eberle, P.C. Sen and L. Yan-Fei "A new resonant gate drive circuit with efficient energy recovery and low conduction loss" *IEEE Industrial Electronics Society*, pp. 650-655, 2005.

[13] N.Z. Yahaya, K.M. Begam and M. Awan "A review on VHF power electronics converter and design issues" *IAENG Engineering Letters*, Vol. 16, Iss. 3, pp. 288-293, Aug. 2008.

[14] K. Yao and F.C. Lee "A novel resonant gate driver for high frequency synchronous buck converter" *IEEE Applied Power Electronics Conference and Expositions*, Vol. 1, pp. 280-286, Mar. 2001.

[15] B. Wang, N. Tipirneni, M. Riva, A. Monti, G. Simin and E. Santi "A resonant drive circuit for GaN power MOSHFET" *IEEE Industry Applications Conference*, pp. 364-368, 2006.

[16] N. Z. Yahaya, K.M. Begam and M. Awan "Switching loss analysis of a diode-clamped resonant gate driver network" *UMS Science and Technology Seminar*, pp. 471-475, Oct. 2008.
[17] P.O. Dwane, D. Sullivan and M.G. Egan "A self-powered resonant gate driver for high power MOSFET module" *IEEE Applied Power Electronics Conference and Expositions*, Vol. 3, pp. 1572-1580, Mar. 2005.
[18] M.H.A. Mashod and N.Z. Yahaya "Design and performance of ZCS-ZVS combined snubber network in DC-DC applications" *IASTED International Conference in Power, Energy and Applications*, pp. 164-169, Sep. 2006.
[19] N.Z. Yahaya and T.M. Dung "Design and improvement of soft-switched quasi-resonant boost converter" *2nd UMS Engineering Conference*, pp. 582-587, Dec. 2008.
[20] H. Yoshihiro, Y. Daichi and K. Hiroyasu "Novel multi resonant ZVS high frequency power converter with high efficiency power conversion" *European Conference on Power Electronics and Applications*, pp. 1-10, Sep. 2005.

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