Adaptive Algorithms Based Cross Talk Reduction Techniques Using Efficient Multipliers in VerilogHDL

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***Abstract*—Crosstalk is a phenomenon by which signals from one channel interfere with the signals of another. In this work, we have investigated the applications of cross talk elimination in interferometer, telecommunications, biomedicine, etc. to improve the performance in these areas. This paper discusses the various algorithms and techniques used to reduce cross talk with their trade-offs. A novel technique is proposed based on performance parameters of different multipliers and FFT method for the analysis of the said algorithms. The hardware utilization of a filter using truncated multiplier is efficient as there is a reduction of 73.64% in hardware with respect to FFT method while with normal cascade network multiplier the reduction is 83.87%.**

***Index Terms*—Adaptive filter, cross talk, fast block least mean square algorithm, fast block least mean square algorithm with distributed arithmetic, FFT, FIR Filter, least Mean square, multipliers.**

I. Introduction

Crosstalk is the phenomenon by which a signal transmitted on one circuit or channel creates an undesired effect in another circuit or channel as shown in Fig. 1. Crosstalk elimination is necessary to increase Signal to Noise Ratio (SNR). It is the undesired effect caused by coupling capacitance of the network. As technology is decreasing in size, we find it all the more important to keep interferences like crosstalk at bay.

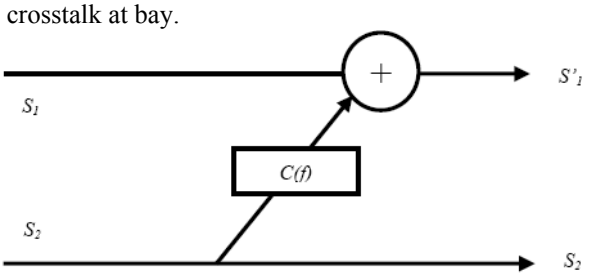

Fig. 1. Crosstalk between two channels [1].

Main elimination techniques involve the phenomenon of digital filtering. Filtering can be either IIR or FIR. According to S. Hernandez-Montero etal [1], an FFT based technique is also proposed which tends to show high performance than linear phase digital filtering for high optimization of FPGA based interferometry which is used to measure the line electron density in plasmas. Adaptive filtering is another field which explores cross talk reduction using different algorithms like Least Mean Square (LMS) [2], Fast Block Least Mean Square (FBLMS) which utilizes FFT and divides the input sequence samples into non-overlapping blocks and Fast Block Least Mean Square with Distributed Arithmetic (FBLMS with DA) where bit level rearrangement takes place for the FFT implementation resulting in multiplier-less architecture at the expanse of adders and memory elements [3]. A study of different multipliers is done as it contributes to the complexity of any filter structure. Based on the performance analysis of these different filters, the desired structure is used to construct the said above elimination techniques and tradeoffs will be observed.

This paper discusses the review on crosstalk reduction techniques and algorithm in Section II while Section III gives an idea regarding design simulation and analysis. Section IV deals with the proposed structure for cross talk elimination and Section V concludes our paper.

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II. Crosstalk Reduction Techniques and Algorithms: A Review

According to the various research papers, we are concerned with the different reduction techniques based on filtering and FFT. Let us analyse the above said reduction techniques and their dependence on the various parameters involved.

A. FIR Filter

FIR filter or Finite Impulse Response filter is a type of digital filter where the filter response to inputs are finite as it settles to zero after a finite amount of time. FIR filters are bounded-input bounded-output (BIBO) stables since output is a sum of finite number of finite multiples of input values.

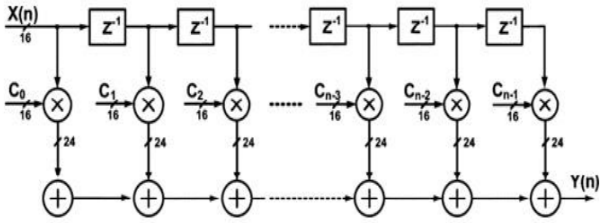

Fig. 2. Conventional FIR filter [1].

According to the Fig. 2, a conventional FIR filter is made up of a delay elements, multipliers and adders. Here C_k values are the coefficients of the filter used for multiplication so that output is equal to the summation of all the delayed samples multiplied by the appropriate coefficients.

$$Y(n) = \sum C(k) \times X(n-k) \quad (1)$$

FIR filters are stable and require no feedback as rounding errors are not compounded which makes implementation simpler. They can be designed for linear phase which makes it appropriate for designing for phase sensitive applications like crosstalk. The main disadvantage of this type of filter over IIR filters is that the power requirement is much higher.

B. Adaptive Filter

Adaptive filter is a filter that self-adjusts its coefficients according to an optimizing algorithm. These algorithms are complex and dependent on the input signals. In some applications where coefficients of a filter are not known, we use an adaptive filter which is based on a feedback technique to modify coefficients depending on the signal received as shown in Fig. 3.

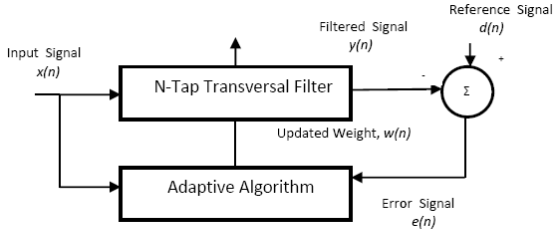

Fig. 3. Adaptive filter [4].

1) Least mean square algorithm (LMS)

This algorithm is based on the principle of updating the filter coefficients by calculating the error in the signals. It actually consists of two part process. First filtered signal is obtained from the input signal from the FIR Transversal Filter used in Fig. 3. This signal is subjected to subtraction from the reference signal to obtain the error signal. The error signal is then subjected to adaptive algorithm for obtaining the updated coefficients of the transversal filter which are later updated [5].

$$y(n)=\sum c(k)\times x(n-k) \quad (2)$$

$$e(n)=d(n)-y(n) \quad (3)$$

$$c(n+1)=c(n)+\mu x(n)\times e(n) \quad (4)$$

Eq. 2 (2) gives the filtered output while the error signal is obtained according to the Eq. 3 (3) Eq. 4 (4) is used by the adapting algorithm to calculate the updated coefficients [2], [7]. LMS algorithm is preferred for its simplicity and the convergence of filter depends on the step size, μ. If μ is small, it takes longer time to converge while for largerμ, the algorithm may never converge [2]. So the performance of filter depends on the step size. Another factor determining the performance is the number of weights of the filter. If filter weights increases, we find that the adders and multipliers used in the structure also increases. Therefore, better care must be given when deciding step size and weights as they are the deciding factor for the performance of an adaptive filter [2].

2) Fast block Lms algorithm (FBLMS)

This is the technique of using LMS algorithm along with FFT technique. In this method, the input sequence is proportioned into non-overlapping blocks of finite length, *P* and these are then applied to a filter of weights *L*, one block at a time. The updated weights are realized using overlap save method using M-point FFT where $M=L+P-1$. It is a fast and efficient algorithm whose hardware complexity comes into play due to the presence of adders and multipliers. It also presents a trade off between efficiency and throughput due to complexity of FFT [3].

3) FBLMS algorithm with distributed arithmetic (FBLMS with DA)

The FBLMS algorithm has low throughput due to complexity of FFT which can be enhanced by implementing distributed arithmetic so as to reduce hardware complexity. This technique of distributed arithmetic results in implementation of FFT without the multiplier hardware by bit level rearrangement of multiply accumulate terms but at the expanse of adders and memory requirement to store pre defined values. As DFT of length *N* has conjugate symmetry, half of the transform is redundant so need not be calculated. Thus further reduction in hardware is obtained using this technique [3]. In this technique, even though hardware reduces power, its consumption is slightly higher than the simple FBLMS adaptive filter. So this method is preferable for higher order filters.

C. FFT Based Architecture

This cross talk elimination architecture was implemented in an FPGA based interferometer for better performance. In this architecture, FFT is the base for the reduction technique as shown in Fig. 4.

The architecture consists of a downsampling stage followed by FFT for the input signals s_m and s_2. The conjugated s_2 signal is multiplied with the other signal and also with itself and further subjected to accumulator.

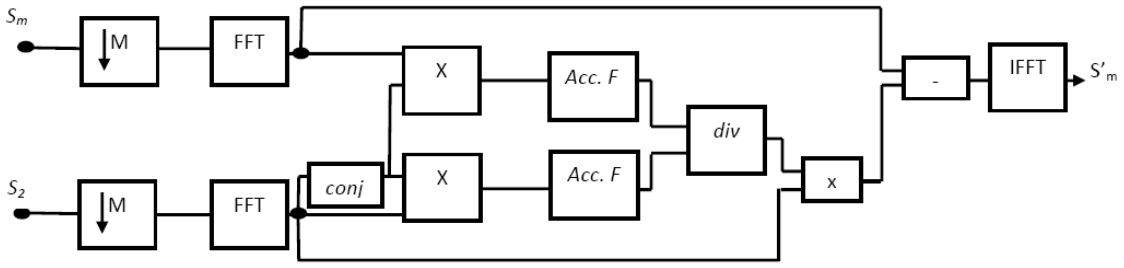

Fig. 4. FFT based architecture [1].

The output from the accumulators after going through a divider block is subjected to multiplier with FFTed s_2 and followed by subtraction with FFTed s_m, The divider block performs conditional operation to extract the estimation. The

estimated signal is then obtained after inverse FFT [1].

III. Design Simulation and Analysis

We are revisiting and comparing the different multipliers like cascade network, tree network, booth algorithm, pipelined architecture [8] and truncated structure [9]-[11] in this paper. From these multiplier structures we construct different filters and analyse its performance with a 4-point butterfly FFT [12]. The analysis is done based on its logic utilization, CPU time, memory usage, delay and power. This work is done using Xilinx ver 12.4 software. The resulting information obtained helps us in proposing a novel cross talk elimination technique.

Logic Utilization. According to Fig. 5 we are able to analyse the logic utilization of filters with different multipliers and FFT method. The analysis provides that the truncated multiplier has the least hardware consumption.

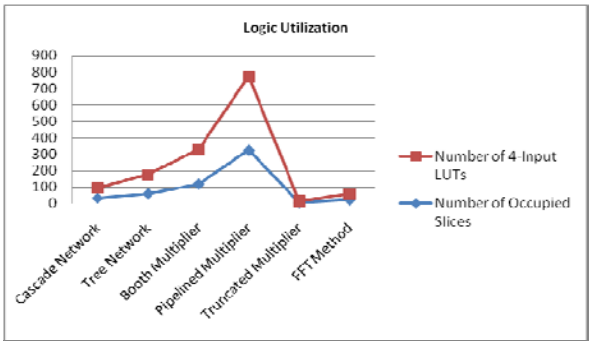

Fig. 5. Logic utilization of different techniques.

Power. For the different filter architectures, we find that the pipelined structure has more power dissipation than the combinational circuit as shown in Fig. 6. As dynamic power is very less compared to static power, we find for smaller structures dynamic power is ignored and only static power dominates.

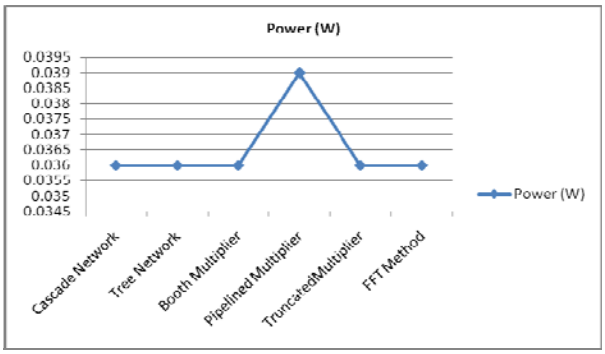

Fig. 6. Power utilization of different techniques.

Memory Usage. Here we are able to analyse the memory usage of different filters implemented and the FFT technique. From the result as shown in Fig. 7, FFT is said to be used in cases where we require less memory while filter using booth multiplier has the highest memory usage.

CPU time and Delay.These factors provide us with the different timing parameters for designing different structures. While the analysis provides that CPU time is less for FFT, the structure with least delay is the pipelined architecture as shown in Fig. 8.

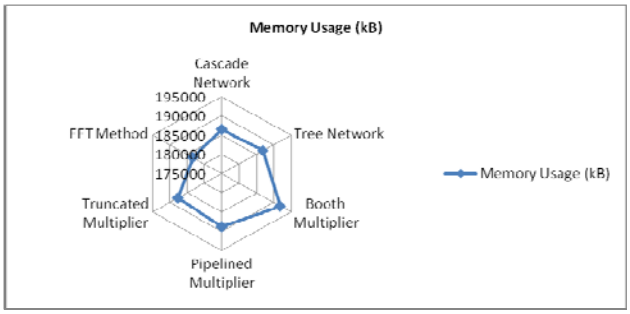

Fig. 7. Memory usage of different techniques.

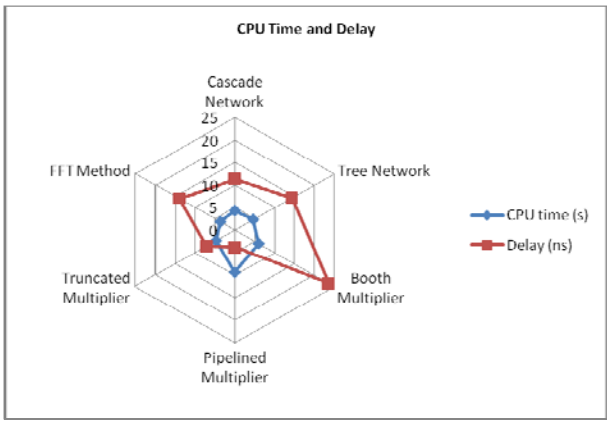

Fig. 8. CPU time and delay of different techniques.

IV. Proposed Structure for Cross Talk Elimination

The proposed work will be used to reduce hardware requirement based on logic utilization. From the analysis, we derive that the filter from truncated multiplier has least hardware. So this filter is used in the various algorithms based on adaptive filtering techniques reviewed. Further analysis will be done with the FFT based architecture of [1] and these algorithms to determine one with better efficiency.

V. Conclusion

Various methods in reducing the cross talk techniques are revisited in this paper. The different techniques applied here are mainly application based and analysed based on the different multiplier architecture. From the analysis of hardware consumption, we can conclude that filter with truncated multiplier is better structure used for cross talk reduction techniques. Different parameters can also be analysed according to our requirement. For future work, we propose to implement this novel filter and analyse the performance of these reduction algorithms.

Acknowledgment

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References

[1] S. H. Montero, J. A. López, M. Sánchez, L. Esteban, and C. A. López, "Real Time FPGA-based crosstalk elimination for multichannel interferometer systems in fusion diagnostics," *IEEE Transactions on Nuclear Science*, July 2013, pp. 1-7.

[2] A. K. Subudhi, B. Mishra, and M. N. Mohanty, "VLSI design and implementation for adaptive filter using LMS algorithm," *International Journal of Computer and Communication Technology*, vol. 2, 2011, pp. 84-88.
[3] S. B. Shivaraj and R. Bhagya, "Design and implementation of adaptive filter for better throughput," *International Journal of Engineering Research and Applications*, vol. 2, no. 3, 2012, pp. 2599-2606.
[4] S. S. Godbole, P. M. Palsodkar, and V. P. Raut, "FPGA implementation of adaptive LMS filter," in *Proc. SPIT-IEEE Colloquium and International Conference*, pp. 2226-2229.
[5] M. Arezki, A. Namane, A. Benallal, P. Meyrueis, and D. Berkani, "Fast adaptive filtering algorithm for acoustic noise cancellation," in *Proc. of the World Congress on Engineering*, vol. II, 2012.
[6] J. Chhikara and J. Singh, "Noise cancellation using adaptive algorithms," *International Journal of Modern Engineering Research*, vol. 2, no. 3, 2012, pp. 792-795.
[7] S. A. Hadei and M. Lotfizad, "A family of adaptive filter algorithms in noise cancellation for speech enhancement," *International Journal of Computer and Electrical Engineering*, vol. 2, no. 2, April 2010.
[8] P. P. Chu, *RTL Hardware Design Using VHDL*, A John Wiley & Sons, Inc., Publication.
[9] R. Devarani and C. S. M. Babu, "Design and implementation of truncated multipliers for precision improvement and its application to a filter structure," *International Journal of Modern Engineering Research (IJMER*), vol. 2, no. 6, 2012 pp. 4736-4742.
[10] M. H. Rais, "Hardware implementation of truncated multipliers using spartan-3AN, virtex-4 and virtex-5 FPGA devices," *American J. of Engineering and Applied Sciences*, vol. 3, 2010, pp. 201-206.
[11] S. R. Rijal and S. G. Mungale, "Design and implementation of 8X8 truncated multiplier on FPGA," *International Journal of Scientific and Research Publications*, vol. 3, no. 3, 2013, pp. 1-5.
[12] A. V. Oppenheim, R. W. Schafer, and J. R. Buck, *Discrete- Time Signal Processing*, Second Edition, Prentice-Hall,Inc.

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