Simulator Based Simplified Design Approach of a CMOS 2-Stage Opamp

Ashis Kumar Mal, Abirjyoti Mondal, Om Prakash Hari, and Rishi Todani

***Abstract*—Two stage (Miller) opamp is one of the most commonly used opamp architectures in analog and mixed signal design. This paper presents the design of a Miller opamp using Potential Distribution Methodology (PDM). It is observed that a wide variety of design objectives depend on distribution of voltages and currents across the differential and gain stage. These dependencies are exploited to optimize the opamp performance and simulation results are presented.**

***Index Terms*—CMOS, opamp, PDM.**

I. Introduction

Analog and mixed signal design has always been a challenging task. Opamps are one of the most important building blocks of analog and mixed signal circuits. Typical opamp design techniques given in literature [1], [2], [3] and even recently published work [4], [5] concentrate mainly on analytical design approach. Being based on SPICE level 1 or level 2 models, the mathematical expressions associated with these techniques are generally simple. However, these expressions are large in number. Young and novice designers may find it difficult to manage so many equations. Alternate design methodologies are also proposed in [6], [7], which handle these equations using other tools like MATLAB, Mathematica, etc. Managing equations may become easier with these tools; however, the design methodology may become extremely complex. When the results obtained by these techniques are used to implement circuits in modern simulator using deep sub-micron devices (which is usually the case), the simulation results do not match with mathematical expectations. This is primarily due to the fact that deep sub-micron devices are modeled using long channel equations. The designer is then forced to adopt a simulator-based approach to optimize the design. Whatever may be the approach; the net time to market increases significantly. PDM is an analog design methodology, which is free from any analytical expression. It directly uses the simulator to arrive to a design point. As the simulator uses the target technology and is capable of handling accurate and complex SPICE models like BSIM, unexpected results or response is avoided.

In PDM, the dimensions of a device are found using a simulator; such that a desired current at pre-defined bias conditions are set. Since the bias conditions are predefined, PDM ensures that all the transistors are in saturation. This methodology can be applied to any analog block and is independent of power supply and technology. In this work, a 2-Stage opamp is designed using PDM. The performance of an opamp is characterized by a number of metrics such as gain bandwidth, phase margin, slew rate, low frequency gain and output swing. These performance metrics are determined by bias currents, component parameters, etc. Further, since opamps are often employed with negative feedback [8], frequency compensation becomes vital for closed loop stability. In order to achieve the required degree of stability, usually indicated by phase margin, other performance parameters are compromised. The following section presents the design approach, simulation results and design optimization techniques.

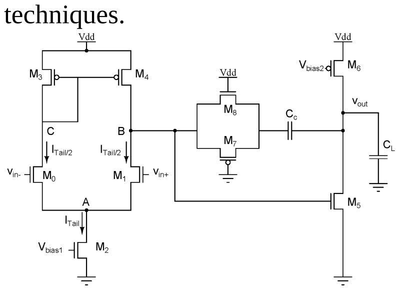

Fig. 1. Schematic of 2-stage miller opamp.

II. Single-Ended 2-Stage Opamp Architecture

Fig. 1 details the architecture of a 2-Stage Miller opamp [8], [9]. The circuit consists of an input differential stage and a common source stage. A compensation capacitor (C_C) provides negative feedback to common source amplifier. Wide Swing Current Mirror shown in Fig. 2, and given in [1], [10], biases the differential and gain stage. This opamp is widely used in a variety of applications such as switched capacitor filters, sensing circuit, analog to digital converters.

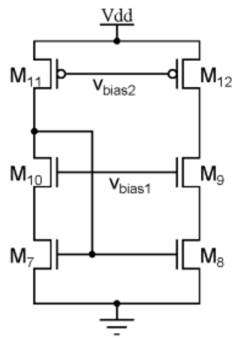

Fig. 2. Schematic of wide swing current mirror

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III. Design of 2-Stage Opamp Using PDM

The 2-Stage opamp is initially designed without much consideration on its performance metrics. Once, the first version of the design is ready, it is modified and optimized to meet the design requirements. PDM uses simulator to find the device dimensions that causes a specified current at pre-defined bias conditions. The bias conditions are chosen such that $V_{DS} \geq V_{GS} - V_T$ keeping $V_{GS} \geq V_T$. Using these conditions, the bias voltages are selected ensuring that the devices remain in saturation. In this work, proprietary 180 nm CMOS process employing BSIM 3v3 model has been used with V_{DD} = 1.8V. The lengths of all transistors are fixed at 500 nm. The design methodology is broken into following steps:

A. Identify Node Voltages

It is desirable to note all the node voltages that are at common mode level (in this case $V_{DD}/2$ or approximately 0.9 V). It is identified that the input nodes (v_{in+} and v_{in-}) and the output node (V_{out}) must be kept at $V_{DD}/2$.

B. Tail Current, I_{Tail}

Slew rate (SR) requirement sets the lower limit of tail current (I_{Tail}) and is given by

$$I_{Tail} = SR \times C_L$$

where C_L is the load capacitance. Half of this tail current ($I_{Tail}/2$) flows through the differential pair transistors, M_0 & M_1. Current mirror shown in Fig. 2 biases M_2 which sets I_{Tail}.

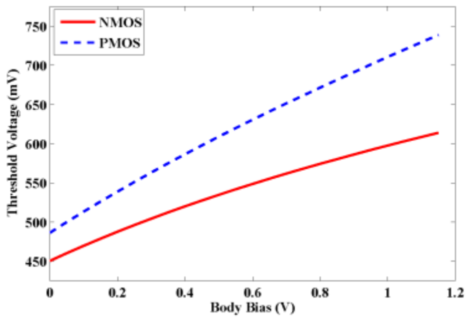

Fig. 3. Effect of body bias on threshold voltage.

C. Threshold Voltage Estimation

It is known that stacking of transistors lead to body bias, which in turn increases threshold voltage of the devices. For proprietary 180nm CMOS process, the effect of body bias on threshold voltage is shown in Fig. 3.

D. Tail Transistor, M_2

The design is started by estimating drop across tail transistor (M_2). It does not experience any body bias and carries a current equal to I_{Tail}. From Fig. 3 its threshold voltage (V_{T0n}) is read as 0.45 V. With overdrive (V_{ov}) of 0.1 V, an appropriate bias voltage of $vb1 = 0.55$ Vis applied to gate. Drain to source drop across tail transistor is kept at 0.3 V. Thus node A is kept at 0.3 V. Thus, for M_2, $V_{GS} = 0.55$ V and $V_{DS} = 0.3$ V. Using simulator a plot of drain current versus transistor width at pre-defined bias conditions is obtained. From this plot, the transistor width corresponding to I_{Tail} is chosen.

E. Differential Pair M_0 and M_1

From Fig. 1 it is noted that gates of M_0 and M_1 are at $V_{CM} = V_{DD}/2$. The source terminal (node A) of these transistors is at 0.3V. Thus the differential pair will have $V_{GS} = 0.6$ V. Due to existence of body bias, threshold voltage (V_{Tn}) of M_0 and M_1 is more than V_{T0n}. V_{Tn} of M_0 and M_1 must be less than V_{GS} with body bias. If not, then the potential at node A is changed accordingly so as to lower body bias and threshold voltage. Since differential pair is fully symmetric between differential inputs, transistor sizes are also fully symmetric. To keep M_1 in saturation, voltage at node B is kept at 0.8 V. Due to systematic offset condition, drain voltage of M_0 is same as that of M_1. Thus for differential pair, $V_{GS} = 0.6$ V and $V_{DS} = 0.5$ V. Therefore, B and C are at 0.8 V.

F. Current Mirror M_3 and M_4

Transistor M_3 is always in saturation because $V_{GD} = 0$. Systematic offset condition implies that drain source (V_{DS}) voltage of M_4 is same as that of M_3. So M_3 is also in saturation. Dimensions of M_3 and M_4 are noted for predefined bias voltages using simulator.

G. Transistor M_5 and M_6

The voltage at node B is applied to gate of NMOS driver (M_5) and an appropriate voltage of 0.6 V to gate of PMOS load (M_6). The output of opamp is fixed at 0.9 V. It is noted that with above set up M_5 and M_6 are in saturation. The dimensions of M_5 and M_6 are obtained using simulator for a current same as I_{Tail} .

H. Compensation Network

Compensation capacitor (C_C) is included in the negative feedback path of the second stage. Its function is to enhance the Miller effect already present in M_5, and thus provide the opamp with a dominant pole. The value of C_C is selected using

$$c_c = 0.22 \times c_L$$

Typically, 2-Stage opamps employ a compensation resistor in series with the compensation capacitor to place a zero on the negative real axis. As per the available literature, the value of this resistor is given by:

$$R \geq \frac{1}{G_{m5}}$$

where, G_{m5} is the transconductance of the second stage. The transconductance of transistors are readily provided by modern simulators. Using this, the value of resistance is first estimated. In this case, $R = 3.7\ \text{K}\Omega$. In this work, the compensation resistor is realized by using transmission gate

(TG). Using TG instead of a resistor makes the design area efficient. Test circuit shown in Fig. 4. is used to estimate the resistance offered by TG. Care is taken that the transistors are operating in linear or triode region and a plot of device dimension versus resistance is obtained as shown in Fig. 5. From this, suitable device dimension is chosen which offers required resistance. When all the device dimensions are found out, the complete opamp schematic is drawn and simulated.

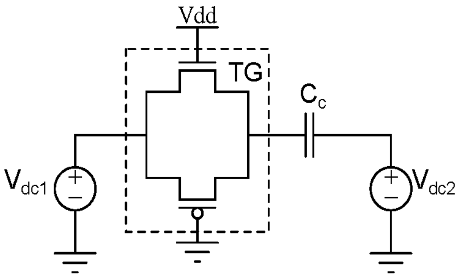

Fig. 4. Test circuit for estimation of resistance using TG.

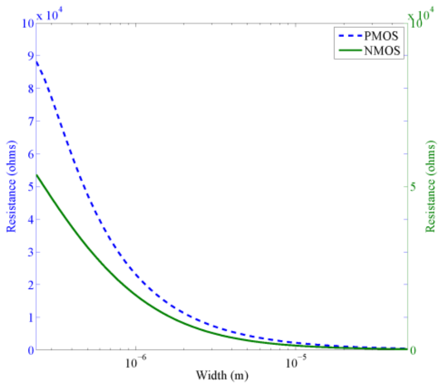

Fig. 5. Plot of resistance versus dimensions.

TABLE I: NODE POTENTIALS AT INITIAL DESIGN

Node	Potentials
A	0.3
B	0.8
C	0.8
V_{in+}	0.9
V_{in-}	0.9
V_{out}	0.9

TABLE II: TRANSISTOR WIDTH AT INITIAL DESIGN (L=500NM)

Transistor	Width (μm)
W2	6.497
W0	3.282
W1	3.282
W3	1.192
W4	1.192
W5	0.8855
W6	1.317

IV. SIMULATION RESULTS AND ANALYSIS

Using the design steps discussed in previous section, a 2-Stage Miller opamp was designed using 180 nm CMOS process employing Cadence Spectre. The current in the tail transistor (M_2) of differential stage was kept at 30 μA. The node potentials at the initial design set up are shown in Table I. The current in the gain stage was fixed at I_{Tail}. Dc analysis results show that all transistors are in saturation and respective dimensions are noted as shown in Table II. AC analysis results with $C_L = 1$ pF and $C_C = 220$ fF is shown in Table III.

TABLE III: INITIAL RESPONSES

Performances	Response
Gain	60.3 dB
Bandwidth	107.6 kHz
Phase margin	62º
UGF	86.41 MHz

V. OPTIMIZATION

The effect of current and voltage distribution across the opamp is now examined. It is found that the performance of the opamp can be optimized in two ways. First, the current distribution between the differential and gain stage, and second, adjusting the potential at nodes A and B.

A. *Current Distribution*

Keeping the node voltages fixed at pre-defined values shown in Table I, currents in M_2 and gain stages are varied in such a way so that total current remains same. Again dc analysis followed by ac analysis is performed for specified current branching. The transistor dimensions are noted along with performance metrics for the same capacitance value. Fig. 6 depicts dependency of DC gain and 3 dB bandwidth (BW) on percentage current entering differential transistors. It is seen that DC gain remains constant whereas BW improves with current branching. Fig. 7 shows the variation of phase margin (PM) and unity gain frequency (UGF) with current branching. Both PM and UGF are decreasing with percentage current entering differential pair. Taking the stability of the opamp into consideration, a suitable current distribution which sets the desired PM may be chosen.

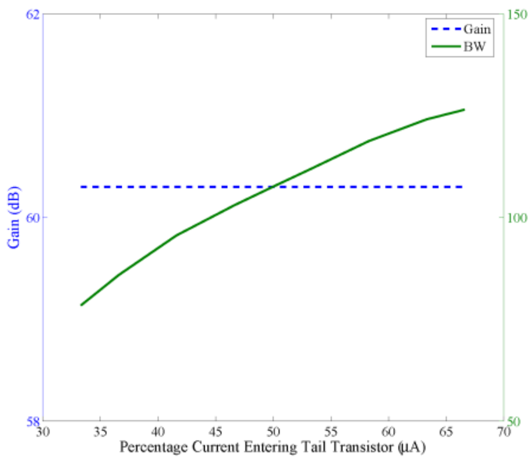

Fig. 6. Gain and 3dB bandwidth dependency.

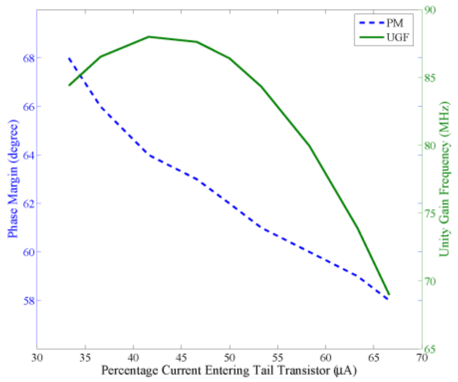

Fig. 7. Phase margin and unity gain frequency dependency.

B. Node Voltage Variation

Further analysis was performed with currents from previous results. Here current is kept fixed at both tail transistor and gain stage while node voltages are varied. The voltages at either of the nodes A or B are varied keeping the other at fixed value. The selection of voltages is done taking into consideration threshold voltage of the transistors and gate bias voltages. After one iteration of analysis, the potential at fixed node is changed to next suitable value. It is kept fixed and variation occurs at other node for the said current only.

C. Potential at Node A

Initially current in M_2 and gain stage was fixed at 30 µA. The voltage at node B was fixed at 0.8 V and node A voltage was varied. Then dc analysis followed by ac analysis is performed for every possible voltage distributions. Transistor dimensions are noted using simulator. Performances are first noted for $C_L = 1$ pF and $C_C = 220$ fF.

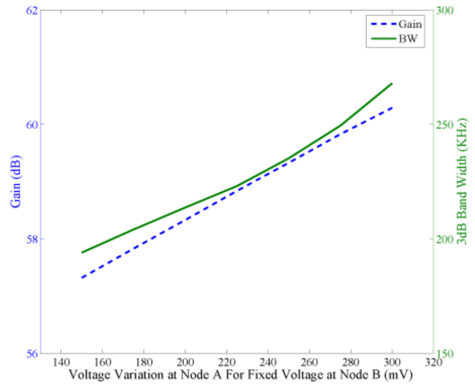

Fig. 8. Gain and 3dB bandwidth dependency.

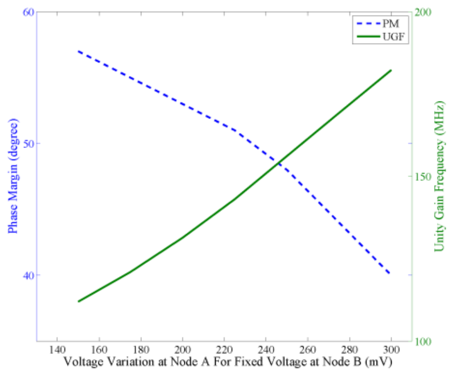

Fig. 9. Phase margin and unity gain frequency dependency.

Then the improved performances are obtained with $C_L = 400$ fF and $C_C = 88$ fF [1]. This process is repeated by specifying a fixed voltage at node B and simultaneously varying node A voltage for same pre-defined current. From Fig. 8-9 it is noted that gain, BW and UGF improves while PM lowers for fixed voltage at node B and variation at node A.

D. Potential at Node B

Now the potential at node A is kept fixed and potential at nodes B is varied. Performances are first noted for default value of capacitances and then improved performances for pre-defined value of capacitances. Fig. 10-11 depicts that gain, PM and UGF are lowering while BW improves for fixed voltage at node A and variation at node B. Although PM is diminishing it is within the limit for a specific voltage distribution mentioned initially so as to attain stability. The optimal results are obtained when drop across the tail transistor is kept at 300 mV, drop across differential pair is around 700 mV and rest drop across PMOS load. It was also observed that same trend in changes occur for the remaining current branching.

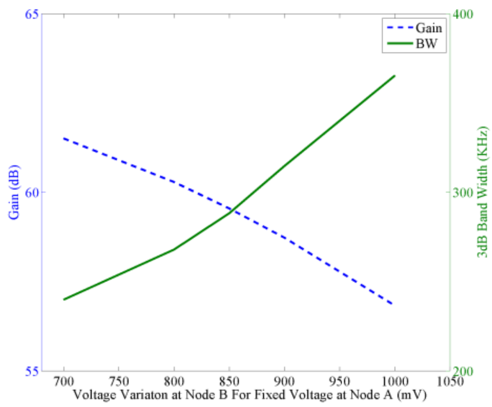

Fig. 10. Gain and 3dB bandwidth dependency.

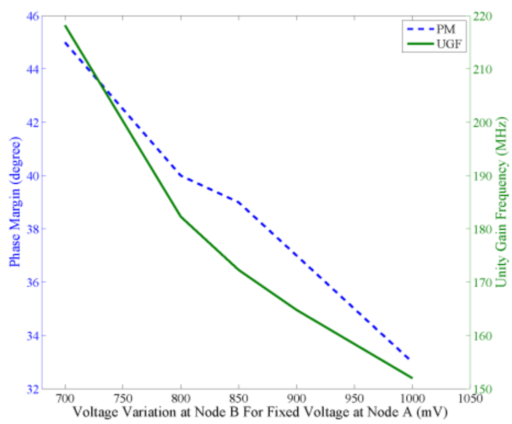

Fig. 11. Phase margin and unity gain frequency dependency

The optimal results for 30 µA current branching are given in Table IV. It is also observed from simulation that if current distribution is increased for pre-defined ratio then better unity gain frequency can be achieved while phase margin is lowered. Minimizing current distribution in same ratio results in improved phase margin and unity gain frequency is degraded.

TABLE IV: PERFORMANCE MEASURES FOR 30 μA IN TAIL PORTION AND NODES A AND B AT 300 MV AND 700 MV RESPECTIVELY

Performances	Initial Performance	Optimized
Gain	60 dB	62 dB
Bandwidth	107.6 kHz	240 kHz
Phase margin	62º	59º
UGF	86.41 MHz	237 MHz

VI. CONCLUSION

PDM is found to be free from complexity of analytical expressions and maintains a simple design methodology, which can be applied to any analog design. So novice designers can implement the steps mentioned previously to design an opamp. Since PDM is independent of supply voltage, process technology and the MOSFET model being used, it can be applied to any complex opamp structures. The results are obtained quickly and are accurate to a greater extent as compared to designs based on analytical equations. The Potential Distribution Method (PDM) proposed earlier is repeated here for the design of 2-Stage Miller opamp and the trade off associated with tail current variations upon performance metric was plotted. It is observed that a specific voltage distribution using PDM results in improved performances and the transistors in saturation, thus simplifying the design process.

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