Characterization of 9T SRAM Cell at Various Process Corners at Deep Sub-micron Technology for Multimedia Applications

R. K. Singh, Shilpi Birla, *Member, IACSIT*, and Manisha Pattanaik

***Abstract*—In the past decades CMOS IC technologies have been constantly scaled down and at present they aggressively entered in the nanometer regime. Amongst the wide-ranging variety of circuit applications, integrated memories especially the SRAM cell layout has been significantly reduced. As it is very well know the reduction of size of CMOS involves an increase in physical parameters variation, this is a factor which has a direct impact on SRAM cell stability. Polysilicon and diffusion critical dimensions (CD) together with implant variations are the main causes of mismatch in SRAM cells. SRAM memory cells have always been designed to occupy the minimum amount of silicon area consistent with the performance and reliability required. Today's system on Chip (SoC) trends result in a major percentage of the total die area being dedicated to memory blocks, consequently making SRAM parameter variations dominate the overall circuit parameter characteristics, including leakage, process variation effects, etc. The reliability is usually measured by static noise margin, SNM [1], and write trip point simulations and measurements. In this paper we have analyzed the stability of the 9T SRAM cell at SS, FF, TT, FS, SF corners. The simulations have been done at 45nm technology.**

***Index Terms*—SOCs, Embedded SRAM, Scaling, Deep submicron level.**

I. Introduction

Subthreshold leakage and gate current are not the only issues that have to be deal at a functional level, but at the same time the power management issues of chips for high-performance circuits such as microprocessors, digital signal processors, and graphics processing units are also necessary. Power management is also a challenge in mobile/multimedia applications. Device variations causing device mismatch for several reasons make the memory more sensitive in terms of stability. For stable read and write, the memory cells must be able to keep the stored state when accessed for reading but quickly change state when accessed for writing. These conflicting needs are even more difficult to achieve with the process variations of sub-100 nm processes.

As the lithography shrinks, the device variations are becoming an ever increasing concern. With the sub-100 nm processes, statistical variations need to be included in the SRAM cell and SRAM block analysis to attain circuit designs with sufficient yield and performance within a defined limited area and power budget.

On the contrary, the transistor and SRAM bit cell size reduction driven by the technology scaling has also made it even more challenging to maintain a sufficient cell stability margin while keeping the same scaling pace of access time and cell size as the mismatching of threshold voltage (Vt) between cross-coupled MOSFET pairs becomes larger and larger [1],[2],[3]. To maintain sufficient margins for read and write stability and read cell current has become challenging as Vdd has to be scaled down in order not only to meet the requirements for device scaling and power savings but also to keep the logic operating voltage compatibility. The Vdd scaling has quickly become one of the most critical challenges because of its strong dependency on the SRAM stability margins for read and write since the invention of 65 nm process node.

In this paper, we have analyzed the stability issues at various process corners of the proposed SRAM cell[14].This 9T SRAM cell has better stability from the earlier publications. In Section II the conventional SRAM along with its limitations has been discussed. In Section III working of the SRAM cell which has been proposed in given. In Section IV the analysis of the cell at various process corners is included in which stability measures like SNM, write margin, read current and leakage has been analyzed and finally the conclusion.

II. Conventional SRAM Cell

The mainstream six-transistor (6T) CMOS SRAM cell is shown in Fig.1 Similarly to one of the implementations of an SR latch, it consists of six transistors. Four transistors (P1, P2, N3, and N4) comprise cross-coupled CMOS inverters and two NMOS transistors, the pass gate transistors or the access transistors N1 and N2 provide read and write access to the cell. Upon the activation of the word line, the access transistors connect the two internal nodes of the cell to the true (BL) and the complementary (BLB) bit lines. A 6T CMOS SRAM cell is the most popular SRAM cell due to its superior robustness, low power and low-voltage operation. Therefore, we will discuss its operation and design in greater detail. An SRAM cell must be designed such that it provides a non-destructive read operation and a reliable write operation. These two requirements impose contradicting requirements on SRAM cell transistor sizing. SRAM cell transistor ratios that must be observed for successful read and write operations are discussed in the following sections.

In the traditional 6T-SRAM (Fig. 1), the cells must be both

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stable (during a read event) and writeable (during a write event) ignoring redundancy; such functionality must be preserved for each cell under worst-case variation. At the cell level, transistor strength ratios must be chosen such that cell static noise margin and write margin are both maintained, which presents conflicting constraints on the cell transistor strengths.

For the cell stability during a read operation, it is desirable to strengthen the storage inverters and weaken the pass-gates. The opposite is desired for cell write ability a weak storage inverter and strong pass-gates. This delicate balance of transistor strength ratios can be severely impacted by device variation, which dramatically degrades stability and write margins, especially in scaled technologies. Low supply voltages further exacerbate the problem as threshold voltage variation consumes a larger fraction of these voltage margins. Variability can thus limit the minimum operating voltage of SRAM. [4]

In a 6T cell, variability tolerances are compromised by the conflicting needs of cell read stability and write ability. Because the same pass-gate devices are used to both read and write the cell, it is inevitable that the two conditions cannot be simultaneously optimized. The 6T SRAM cell stability problems also arise during a write operation to an unselected column when the word line is activated while both bit lines are held high [4],[5]. A situation that produces equivalent bias conditions to a read operation. So, different topologies of SRAM cell have been implemented at various technologies to improve the data stability and leakage power consumption.

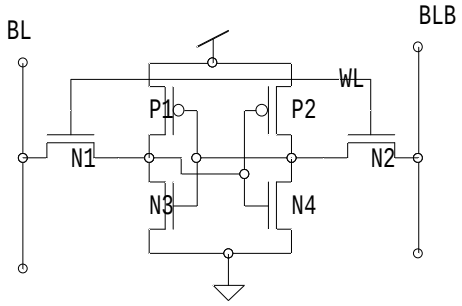

Fig. 1. 6T SRAM cell

III. Analysis of the 9T SRAM Cell

Many new cell topologies have been proposed for stability improvement like 7T, 8T, 9T, 10T, 11T.Although each has some advantages and disadvantages along with them. Various topologies of SRAM cell has been introduced, 7T SRAM cell in which a read static noise margin is achieved by cutting off a pull down path during read operation but has limited write capability due to single end write operations [6], [7].8T SRAM cell which is one of the popular topology which increases the stability but has its own limitation. In this paper the limitation of 8T has been removed and alternative topologies have been discussed to increase the stability.

A 7T cell [34] achieves read-static-noise-margin-free by cutting off a pull-down path during read operations, but has limited write capability due to single-end write operations. A read-decoupled (RD) 8T cell [8], [9], [10], [11], which isolates its read-port from the storage node, is a popular solution for many low-VDD chips because of its superior read stability. However, RD-8T cells do not significantly increase the write margin (WM), and still suffer from half-select stability failure during a write operation. Divided wordline schemes prevent disturbance at half-select cells, but do not solve write failures.

In this section, we describe our cell design in Fig. 2. As mentioned previously, it is composed of two cross coupled P-P-N inverters, and data is stored in node Q and node Qb in a complementary manner. Transistors P1, PP3, and ND1 form a P-P-N inverter and P1, PP4, ND2 form another.[12]

ND1 provides the read current path for discharging a bitline (BL) or its complementary (BLB), depending on the stored values of Q and Qb, respectively. The source terminal of this transistor is connected to the VGND pin, which connects to the ground voltage only during the read operation. Anytime else, it stays high to curb unnecessary leakage current.V1 and V2 are located between the two cascaded P-MOS transistors forming the P-P-N inverter. Q and Qb are the storage nodes .BL and BLB are bitlines while WL is the word line as in conventional 6T SRAM cell.[12]

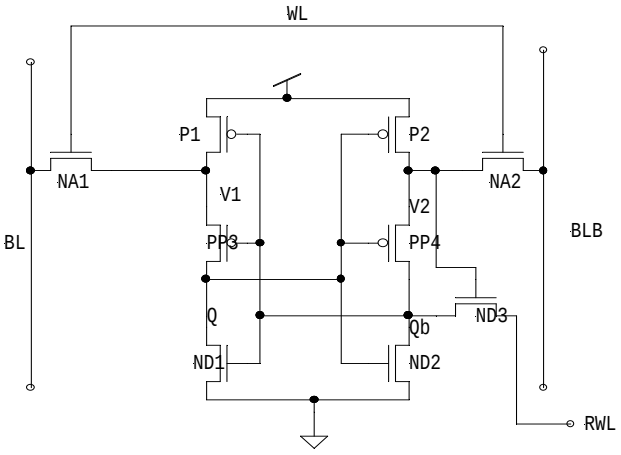

Fig. 2. Proposed SRAM Cell

IV. Process Corner Analysis

A process corner is an example of a design-of-experiments (DoE) technique that refers to a variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer. Process corners represent the extremes of these parameter variations within which a circuit that has been etched onto the wafer must function correctly. A circuit running on devices fabricated at these process corners may run slower or faster than specified and at lower or higher temperatures and voltages, but if the circuit does not function at all at any of these process extremes the design is considered to have inadequate design margin.

There are therefore five possible corners: typical-typical (TT) (not really a corner of an n vs. p mobility graphs, but called a corner, anyway), fast-fast (FF), slow-slow (SS), fast-slow (FS), and slow-fast (SF). The first three corners (TT, FF, SS) are called even corners, because both types of devices are affected evenly, and generally do not adversely affect the logical correctness of the circuit. The resulting devices can function at slower or faster clock frequencies, and are often binned as such. The last two corners (FS, SF)

are called "skewed" corners, and are cause for concern.

The most common measure of checking the stability is the butterfly curve from which we can get the Static Noise Margin which is the amount of maximum tolerable DC noise voltage without disturbing the output [13]. Other alternate stability methods have also been reported in [14], [15] which is N curve .The N curve is used to get the read stability and write stability but here we have used the conventional method for finding the stability measures.

A. *SNM at Various Process Corners*

We have analyzed the SNM at different process corners .We have vary the voltages and temperature as in Fig.3 so that we can analyze the effects of voltage and temperature also on the stability. From Fig.3, Fig.4, Fig.5 we can observe that as Vdd is scaled down the SNM also decreases. From Fig.6 we can see that the Noise Margin decreases as temperature increases and the circuit observed the SNM at all the corners.

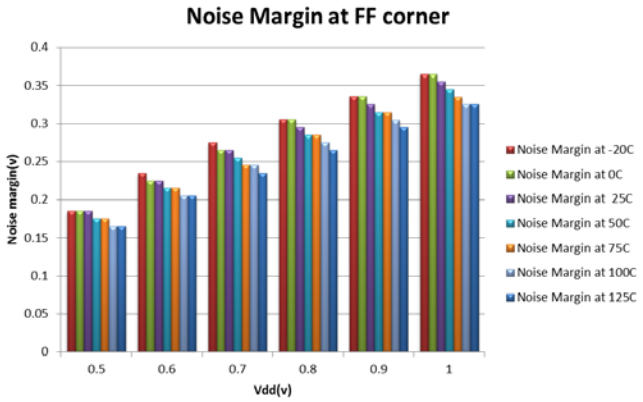

Fig. 3. Noise Margin at FF corner

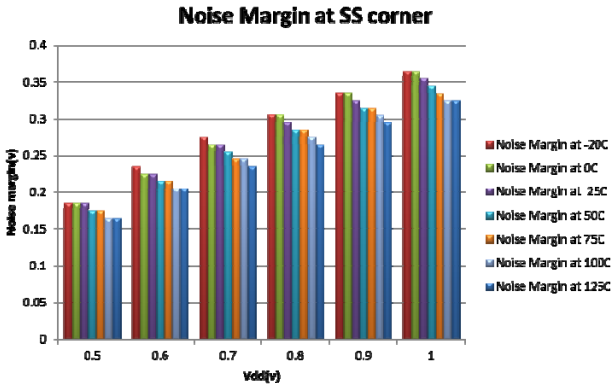

Fig. 4. Noise Margin at SS corner

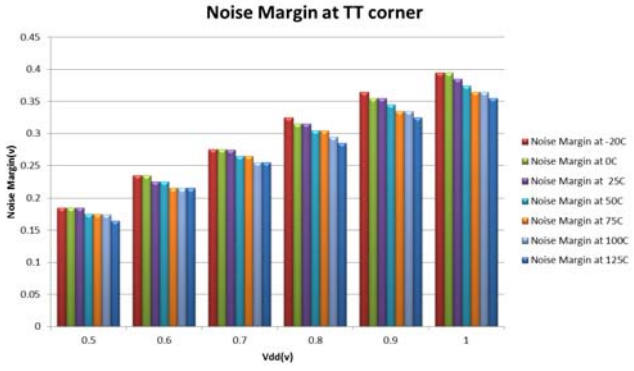

Fig. 5. Noise Margin at TT corner

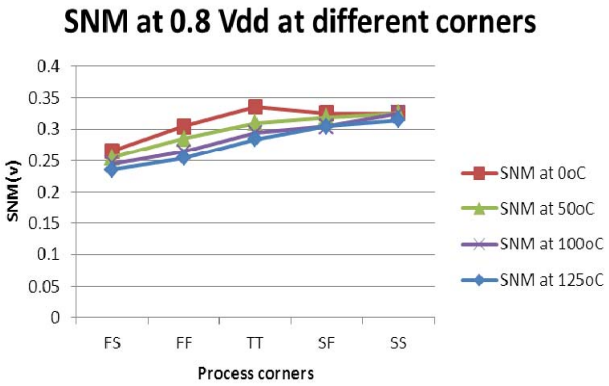

Fig.6 SNM at different corners

B. *Write Margin at Various Process Corners*

The write margin (WRM) is defined as the rest of potential difference between the BL level at which the data is flipped and the end-point (e.g., GND).

Write margin is also analyzed at various process corners and we have taken Vdd=0.8V and analyzed the effect of temperature and process corners on write margin. The SNM decreases with the temperature but in case of write margin it is just reverse here increase in the temperature decreases the Write Margin. As in the Fig.7 we can see that the minimum write margin is observed in case of SF corner and the maximum write margin at FS corner. The cell operates in all the corners.

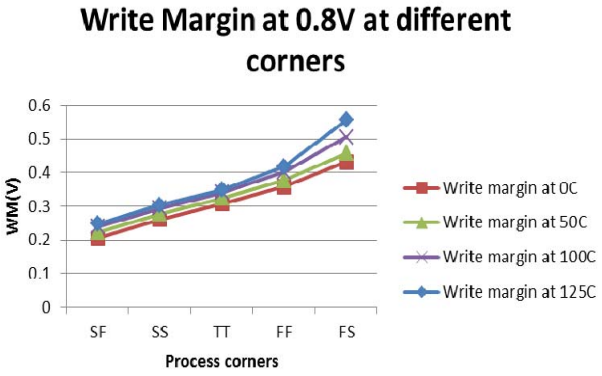

Fig. 7. Write Margin at different corner

C. *Read Current*

For minimum read delay the widths of both devices should therefore be as wide as possible. While SNM evaluate cell functionality, the cell read current, 'Iread' is a major component in designing array access time. Read current is also a measure of the stability and we have analyzed the read current at Vdd=0.8V at different temperatures and process corners as shown in Fig.8. The V DD scaling has quickly become one of the most critical challenges because of its strong dependency on the SRAM stability margins for read and writes stability. Temperature affects the read current inversely with respect to write margin. It decreases with increase in the temperature; it has maximum value at FF corner.

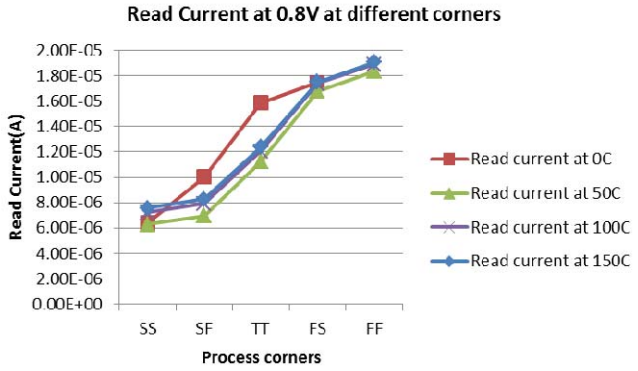

Fig. 8. Read current at different corners.

D. Leakage Current

Power consumption is one of the most important factors in multimedia applications as the requirement is of ultra-low power consumption. As the temperature increases the leakage also increases and we can see that at FF corner the leakage is highest as in Fig.9. The current measurement is done at Vdd =0.8V.The worst case leakage was 7.49nA.

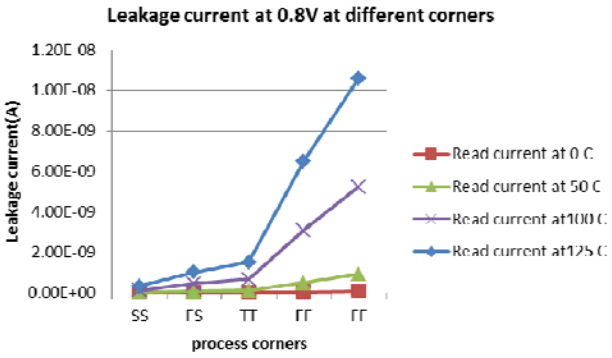

Fig.9 Leakage current at different corners

V. Conclusion

In this paper we have analyzed the 9T SRAM cell which has been proposed in [14].The cell has been analyzed at various process corners to check the read and write stability. We have taken Vdd=0.8V.On analyzing the the various corners we see that the highest SNM is at TT corner and the highest Write Margin is at FS and Read Current is at FF corner. But the cell has highest leakage at FF corner so the process corner. But the cell has operation at all the process corners and it shows good response at TT and FS and FF corners which is required for measuring the cell stability. SNM of the cell is 0.33V, Write Margin is 0.35 V and Read current is 14µA at Vdd=0.8V and temperature is 50°C.These values are better in respect to other published SRAM 9T Cell and the cell area is 1.85x 1.02 μm^2.

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