Crosstalk Interconnect Noise Optimization Technique Using Wire Spacing and Sizing for High Speed Integrated Circuits

P. V. Hunagund and A. B. Kalpana

***Abstract*—Scaling the minimum feature size of VLSI circuits to sub-quarter micron and its clock frequency to 3GHz has caused crosstalk noise to become a serious problem that degrades the performance and reliability of high speed integrated circuits. This paper presents an efficient method for computing the capacitive crosstalk in sub-quarter micron VLSI circuits. In this paper, we present a complete analytical crosstalk noise model which incorporates all physical properties including victim and aggressor drivers, distributed RC characteristics of interconnects and coupling locations in both victim and aggressor lines. We present closed-form analytical expressions for peak noise and noise width to estimate on-chip crosstalk noise and also shown that crosstalk can be minimized by wire spacing and wire sizing optimization technique. These models are verified for various deep submicron technologies.**

***Index Terms*—Aggressor, Coupling, Crosstalk, Interconnect noise, Wire spacing,**

I. Introduction

Advancement in the field of very large scale integration (VLSI) have lead to a decrease in device geometries (deep submicron technology), high device densities, high clock rates, and thus small signal transition times. Thus, interconnection lines that were once considered to be electrically isolated can now interfere with each other and have an important impact on system performance and correctness. One such interaction caused by parasitic coupling between wires is known as crosstalk. If not carefully considered during design validation, crosstalk can cause extra signal delay, logic hazards, and even circuit malfunction. Accurate modeling and simulation of interconnect delay due to crosstalk thus becomes increasingly important in the design of high-performance integrated circuits.

The net on which noise is being induced is called the *victim* net whereas the net that induces this noise is called the *aggressor* net. Crosstalk noise not only leads to modified delays [2],[3] but also to potential logic malfunctions [4],[5]. To be able to deal with the challenges brought by this recently emerging phenomenon, techniques and tools to estimate and avoid crosstalk noise problems should be incorporated into the IC design cycle from the early stages. Any such tool requires fast yet accurate crosstalk noise models both to estimate noise and also to see the effects of various interconnect and driver parameters on noise. Several papers, which propose crosstalk models, can be found in recent literature. In [6], telegraph equations are solved directly to find a set of analytical formulae for peak noise in capacitively coupled bus lines. [7] derives bounds for crosstalk noise using a lumped model but assuming a step input for aggressor driver. The peak noise expression in [7] is extended by [8],[9] to consider a saturated ramp input and a π circuit to represent the interconnect. These models fail to represent the distributed nature of the interconnect. In [10], an Elmore delay like peak noise model is obtained for general RC trees but it assumes an infinite ramp input. This assumption causes the model to significantly overestimate peak noise, especially for small aggressor slews, which is very likely to occur in today's deep submicron designs. Devgan's metric has been improved in [11]. Interconnect crosstalk can be modeled and minimized using different techniques [14],[15].

In this paper, a much improved crosstalk noise model, called the 2π- model is discussed. It overcomes major drawbacks of existing models by taking into consideration many key parameters, such as the aggressor slew at the coupling location, the coupling location at the victim net (near-inverter or near-receiver), and the coarse distributed RC characteristics for victim net. It includes simple *closed-form* expressions to estimate both *peak noise* and *noise width* and provides very clear physical meaning for key noise contribution terms. All these characteristics of model 2π make it ideal to guide noise-aware layout optimizations explicitly. It is also shown that crosstalk can be minimized by various other optimization techniques [18],[19].

II. An Improved 2Π Crosstalk Noise Model

A. 2-π Model and its Analytical Waveform

For simplicity, we first explain 2-π model for the case where the victim net is an RC line. We will extend the 2-π model to a general RC tree in Section 2.3. For a victim net with some aggressor nearby, as shown in Fig. 1(a), let the aggressor voltage pulse at the coupling location be a saturated ramp input with transition time (i.e., slew) being t_r and the interconnect length of the victim net before the coupling, at the coupling and after the coupling be L_s, L_c and L_e, respectively. The 2-π type reduced RC model is generated as shown in Fig. 1(b) to compute the crosstalk noise at the receiver. It is called 2-π model because the victim net is modeled as two π-type RC circuits, one before the coupling and one after the coupling. The victim driver is modeled by effective resistance R_d, Other RC parameters C_x, C_1, R_s, C_2, R_e, and C_L are computed from the geometric information from

Manuscript received September 19, 2011; revised December 3, 2011.

P. V. Hunagund is with the Department of Applied Electronics, Gulbarga University, Gulbarga, India (e-mail:prabhakar.hunagund@gmail.com).

A. B. Kalpana is with the Electronics and Communication Engineering Department, Bangalore Institute of Technology, Bangalore, India (e-mail: abkalpana@gmail.com).

Fig. 1(a) in the following manner. The coupling node (node 2) is set to be the center of the coupling portion of the victim net, i.e., $L_s + L_c/2$ from the source. Let the upstream and downstream interconnect resistance capacitance at Node2 be R_s/C_s and R_e/C_e, respectively. Then capacitance values are set to be $C_1 = C_s/2$, $C_2 = (C_s + C_e)/2$ and $C_L = C_e/2 + C1$. Compared with [12],[13]which only used one lumped RC for the victim net, it is obvious that our *2-π* model can model the *coarse* distributed RC characteristics. In addition, since we consider only those *key* parameters, the resulting 2-π model can be solved analytically.

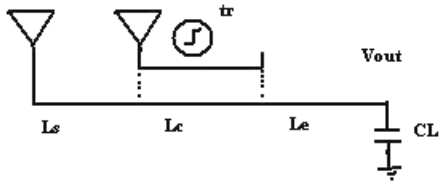


Fig. 1(a). The layout of a victim net and aggressor above it

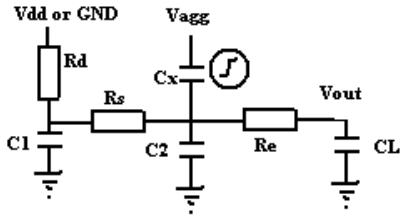


Fig. 1(b). The 2π crosstalk noise model.

From Fig. 1(b), we have the impedance at node 1, Z_1 Satisfying the following

$$\frac{1}{Z_1} = \frac{1}{R_d} + sC_1$$

Then the s-domain voltage at node 2 by $V_2(s)$, then

$$V_2(s) = \frac{Z_2}{Z_2 + \frac{1}{sC_L}} . V_{agg}(s)$$

The output voltage V_{out} in the s-domain is

$$V_{out}(s) = V_2(s) . \frac{\frac{1}{sC_L}}{R_e + \frac{1}{sC_L}} \tag{1}$$

Substituting Z_1, Z_2 and V_2 into $V_{out}(s)$, we have

$$V_{out}(s) = \frac{a_2 s^2 + a_1 s}{s^3 + b_2 s^2 + b_1 s + b_0} . V_{agg}(s) \tag{2}$$

Writing the transfer function $H(s)$ into the poles/residues form:

$$H(s) = \mathrm{V_{out}}(s) = \frac{a_2 s^2 + a_1 s}{s^3 + b_2 s^2 + b_1 s + b_0} \equiv \frac{k_1}{s - s_1} + \frac{k_2}{s - s_2} + \frac{k_3}{s - s_3}$$

The three poles s_1, s_2 and s_3 are the three roots of $s^3+b_2s^2+b_1s+b=0$, which can be obtained analytically using standard mathematical techniques (details omitted due to page limitation). After each pole/residue pair is obtained, its corresponding time domain function is just $f_i(t)=k_i e^{s_i t}$ *(i =* 1,2,3*)*.

For the aggressor with saturated ramp input and its Laplace transformation is

$$V_{agg}(s) = \frac{1 - e^{-st_r}}{s^2 t_r} \tag{3}$$

Then for each pole/residue pair, the s-domain output $V_{out}(s) = \frac{k_i}{s - s_i} V_{agg}(s)$ and its inverse Laplace is

$$= \begin{cases} -\frac{k_i(1 + s_i t)}{s^2 t_r} + \frac{k_i e^{s_i t}}{s^2_i t_r} & 0 \le t \le t_r \\ -\frac{k_i e^{s_i (t - t_r)}}{s_i^2 t_r} + \frac{k_i e^{s_i t}}{s^2_i t_r} + \frac{k_i}{s_i} & t \ge t_r \end{cases} \tag{4}$$

Therefore, the final noise voltage waveform is simply the summation of the voltage waveform from each pole/residue pair

$$v_{out}(t) = v_{out1}(s) + v_{out2}(s) + v_{out3}(s) \tag{5}$$

The 2-*π* model has been tested extensively and its waveform from (5) can be shown to be almost identical compared to HSPICE simulations.

B. Closed-Form Noise Amplitude and Width

When although the closed-form noise waveform has been derived in the previous subsection, the solution by itself is still quite complicated. Moreover, it provides little intuition about some key measurements for crosstalk noise, such as noise peak amplitude and noise width, which are very important to guide noise reduction by interconnect optimizations. Simple closed-form expressions for these measurements are highly desired, since they provide more insight about how various interconnect parameters affect the crosstalk noise and to what extent. In this subsection, we will further simplify the original *2-π* model and derive closed-form formulae for noise amplitude and noise width.

Using dominant-pole approximation method in a similar manner like [14], [15], [16], we can simplify (2) into

$$V_{out}(s) \approx \frac{a_1 s}{b_1 s + b_0} . V_{agg}(s) = \frac{t_x \left(1 - e^{-st_r}\right)}{st_r (st_v + 1)} \tag{6}$$

where the coefficient are

$$t_x = (R_d + R_s) C_x \tag{7}$$

$$t_v = (R_d + R_s)(C_x + C_2 + C_L) + (R_e C_L + R_d C_1) \tag{8}$$

It is interesting to observe that t_x is in fact the RC delay term from the upstream resistance of the coupling element times the coupling capacitance, while t_v is the distributed Elmore delay of victim net.

We will further discuss their implications later computing the inverse Laplace transform of (6). We can obtain the following simple time domain waveform

$$v_{out} = \begin{cases} \frac{t_x}{t_r} \left(1 - e^{-\frac{t}{t_v}}\right) & 0 \le t \le t_r \\ \frac{t_x}{t_r} \left(e^{-\frac{(t - t_r)}{t_v}} - e^{-\frac{t}{t_v}}\right) & t > t_r \end{cases} \tag{9}$$

It is also interesting to compare with the recent work by [17], where the peak noise with saturated ramp input can be

written as $v'_{max} = t_x/(t_v+t_r/2)$. (10)

Although obtained from a totally different approach, v'_{max} from [17] is indeed a first-order approximation of our v_{max} in (10), since However, such approximation is only when $t_r<t_v$. It will be much off when $t_r >> t_v$. This explains why v'_{max} in [17] gives twice peak noise.

Peak noise amplitude V_{max} is not the only metric to characterize noise. Under some circumstance, even the peak noise exceeds certain threshold voltage, a receiver may still be noise immune. This can be characterized by some noise amplitude versus width plots. The noise width is defined as follows.

$$\frac{t_x}{t_r}\left(1 - e^{-\frac{t_r}{t_v}}\right) = \frac{t_x}{t_v}\left[1 - \frac{1}{2}\frac{t_r}{t_v} + ...\right] \quad (11)$$

$$\approx \frac{t_x}{t_v}\frac{1}{1+\frac{1}{2}\frac{t_r}{t_v}} = \frac{t_x}{t_v + \frac{t_r}{2}} \quad (12)$$

Definition 1 Noise Width: Given certain threshold voltage level v_t, the noise width for a noise pulse is defined to be the length of time interval that noise spike voltage v is larger or equal to v_t.

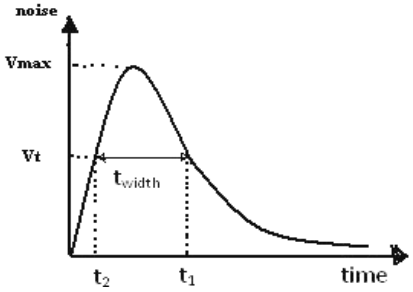


Fig. 2. Illustration of the noise width

From Eq. (9), we can compute t_1 and t_2, and thus the noise width

$$t_2 - t_1 = t_v \ln\left[\frac{(t_x - t_r v_t)\left(e^{t_r/t_v} - 1\right)}{t_r v_t}\right] \quad (13)$$

In this paper, we set the threshold voltage v_t to be half of the peak noise voltage, $v_t=v_{max}/2$. Then the noise width of (13) is simplified into

$$t_{width} = t_2 - t_1 = t_r + t_v \ln\left[\frac{1 - e^{-2t_r/t_v}}{1 - e^{-t_r/t_v}}\right] \quad (14)$$

As for the time complexity, since we have the closed-form expressions for the poles, residues, and waveform for each pole/residue pair, the computation time for transfer function and waveform for a given 2-π model can be done in constant time. To reduce the original circuit to the 2-π model, we only need a linear traversal (to compute upstream downstream interconnect resistance/capacitance at the coupling node) of the victim net, which can be done in linear time as well as in [12],[18]. It is obviously the lower bound of the computational complexity for any reasonable noise model.

III. Noise Avoidance Technique

A general case for two coupled lines is shown in Fig. 3. Both aggressor and victim lines are divided into 3 regions: interconnect segment before coupling location, coupling location and interconnect segment after coupling location. These regions of aggressor and victim lines are represented by L_{al}, L_c, L_{ar}, L_{vl} and L_{vr} as seen in the Fig. 3. We propose the linear model shown in Fig.4, to compute crosstalk noise at the receiver of victim net. Victim driver is modeled by effective holding resistance R_h, whereas aggressor driver is modeled by an effective Thevenin model consisting of a saturated ramp voltage source with a slew rate of t_r and the Thevennin resistance R_{th}. Other components of our model are computed based on the technology and geometrical information obtained from Fig. 3. Coupling node (node 2 in aggressor net and node 5 in victim net) is defined to be the middle of coupling location for both nets, i.e. $L_{al} + L_c/2$ away from aggressor driver and $L_{vl} + L_c/2$ away from the victim driver. For the aggressor net, let the upstream and downstream resistance-capacitance at node 2 be R_{a1}-C_{au} and R_{a2}-C_{ad} respectively. Then, $C_{a1} = C_{au}/2$, $Ca2 = (C_{au}+C_{ad})/2$ and $C_{a3} = C_{ad}/2+C_{la}$. Similarly for the victim net, let the upstream and downstream resistance capacitance pair at node 5 be R_{v1}-C_{vu} and R_{v2} -C_{vd} respectively. Then, $C_{v1} = C_{vu}/2$, $C_{v2} = (C_{vu} + C_{vd})/2$ and $C_{v3} = C_{vd}/2 + C_{lv}$.

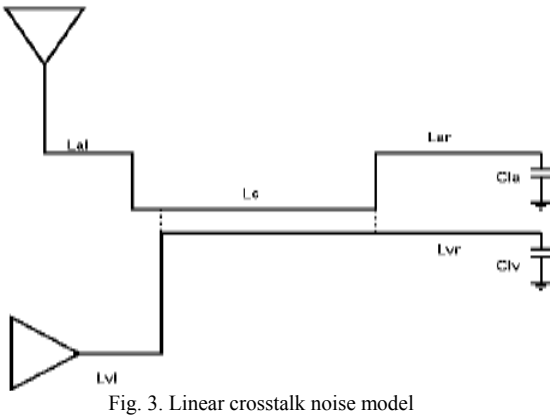


Fig. 3. Linear crosstalk noise model

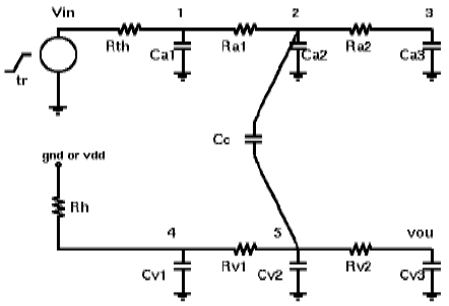
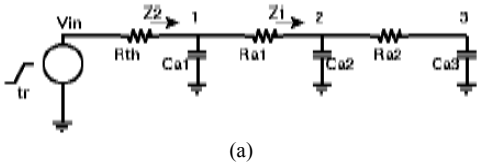
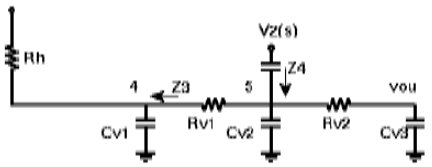


Fig. 4. Linear crosstalk noise model

To simplify the analytical calculation of transfer function $H(s)$ from V_{in} to V_{out}, we initially decouple the aggressor line from victim line (Fig.5(a)), and compute the transfer function from V_{in} to V_2. We then apply $V_2(s)$ to the victim line as seen in Fig. 5 (b). This assumption is valid when victim line is not loading aggressor line at node 2 significantly.



(a)



(b)

Fig. 5. Decoupled model to calculate transfer Function.

A. Wire Spacing

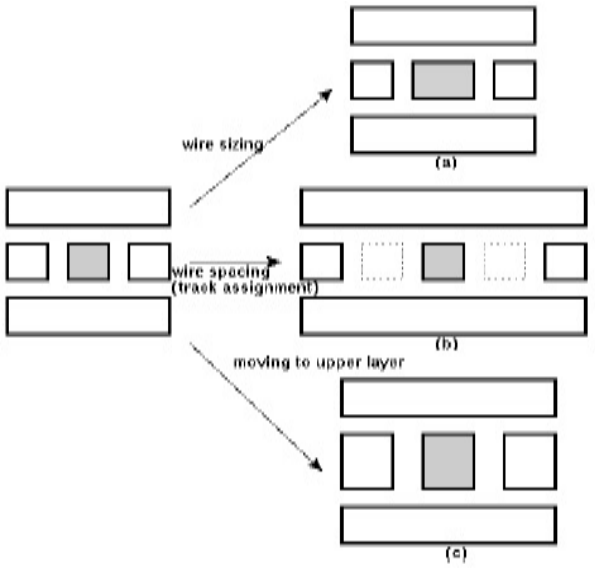


Fig. 6. Cross-section of victim line and surroundings

For a wire of fixed width, its coupling capacitance decreases while its ground capacitance increases, as its spacing to a neighbor wire increases. The decreasing of coupling capacitance is easily explained by the inverse relation between capacitance and distance. Increasing of ground capacitance is due to the fact that as spacing between two wires increases, some of the field lines contributing to coupling capacitance fail reaching the neighbor wire and start contributing to ground capacitance (Fig. 6(b)). From our model,

$$\frac{\delta v_{peak}}{\delta C_C} = \left(\frac{R_h + R_{v1}}{t_r}\right)\left(1 - e^{-t_r/t_v}\right) - \frac{(R_h + R_{v2})^2 C_C}{t_v^2} e^{-t_r/t_v} \quad (15)$$

$$\frac{\delta v_{peak}}{\delta C_{v1}} = \frac{-(R_h + R_{v1}) C_C R_h}{t_v^2} e^{-t_r/t_v} \quad (16)$$

$$\frac{\delta v_{peak}}{\delta C_{v2}} = \frac{-(R_h + R_{v1})^2 C_C}{t_v^2} e^{-t_r/t_v} \quad (17)$$

$$\frac{\delta v_{peak}}{\delta C_{v3}} = \frac{-(R_h + R_{v1}) C_C (R_h + R_{v1} + R_{v2})}{t_v^2} e^{-t_r/t_v} \quad (18)$$

$$\frac{\delta v_{peak}}{\delta C_{a1}} = \frac{-(R_h + R_{v1}) C_C R_{th}}{t_v^2} e^{-t_r/t_v} \quad (19)$$

$$\frac{\delta v_{peak}}{\delta C_{a2}} = \frac{-(R_h + R_{v1}) C_C (2R_{a1} + R_{th})}{t_v^2} e^{-t_r/t_v} \quad (20)$$

$$\frac{\delta v_{peak}}{\delta C_{a3}} = \frac{-(R_h + R_{v1}) C_C (2R_{a1} + 2R_{a2} + R_{th})}{t_v^2} e^{-t_r/t_v} \quad (21)$$

From Eq.(15), $\delta v_{peak}/\delta C_C$ is positive but diminishes when $t_v >> t_r$ in which case reduction in coupling capacitance doesn't help peak noise reduction. Eqn's (16, 17, 18, 19, 20, 21) show that an increase in the ground caps of both victim and aggressor lines help reduce noise on the victim net. Their relative effectiveness's are as follows.

$$\frac{\delta v_{peak}}{\delta C_{v3}} < \frac{\delta v_{peak}}{\delta C_{v2}} < \frac{\delta v_{peak}}{\delta C_{v1}} < 0 \quad (22)$$

$$\frac{\delta v_{peak}}{\delta C_{a3}} < \frac{\delta v_{peak}}{\delta C_{a2}} < \frac{\delta v_{peak}}{\delta C_{a1}} < 0 \quad (23)$$

As can be seen from (22 - 23), for the same amount of increase in ground capacitance, peak noise reduction is most effected from near sink capacitances in both victim and aggressor lines.

B. Wire Sizing

As a wire's width is increased, its resistance decreases and its ground capacitance increases (Fig. 6(a)). If we look at how noise peak is affected by changes in interconnect resistances, we get the following sensitivities from our model.

$$\frac{\delta v_{peak}}{\delta R_{v1}} = \frac{C_C}{t_r}\left(1 - e^{-t_r/t_v}\right) - (R_h + R_{v1})\frac{C_C (C_C + C_{v2} + C_{v3})}{t_v^2} e^{-t_r/t_v} \quad (24)$$

$$\frac{\delta v_{peak}}{\delta R_{v2}} = \frac{-(R_h + R_{v1}) C_C C_{v3}}{t_v^2} e^{-t_r/t_v} \quad (25)$$

$$\frac{\delta v_{peak}}{\delta R_{a1}} = \frac{-2(R_h + R_{v1}) C_C (C_{a2} + C_{a3})}{t_v^2} e^{-t_r/t_v} \quad (26)$$

$$\frac{\delta v_{peak}}{\delta R_{a2}} = \frac{-2(R_h + R_{v1}) C_C C_{a3}}{t_v^2} e^{-t_r/t_v} \quad (27)$$

Equation (24) shows that the effect of R_{v1} on noise reduction is very similar to that of R_h. On the other hand, from Equations (25, 26, 27), the effects of R_{v2}, R_{a1} and R_{a2} are opposite.

Peak noise increases as these resistances are decreased. As a result, when a victim wire's width is increased, the change in peak noise depends on Eqn's (16, 17, 18, 25, 26). Eqn's (25 and 26) show the importance of coupling location on how effective wire sizing will be. If the coupling location is close to victim driver, Eq.(26) will be more effective than Eq. (25) and thus effect of wire sizing on noise reduction will diminish. Wire sizing will be most effective when coupling location is close to victim receiver.

On the other hand, the effect of increasing an aggressor wire's width depends on relative magnitudes of $\delta v_{peak}/\delta C_{ai}$ and $\delta v_{peak}/\delta R_{ai}$. By looking at Eqn's (19, 20, 21, 26, 27), it can be seen that the capacitance sensitivities are greater in magnitude than resistance sensitivities. Thus if R_{ai} decrease as much as C_{ai} increase as a result of width increase, this will help reduce noise on the victim receiver input. For validation interconnect parameters are considered from 32nm and 55nm technologies. Output voltages are observed for normal driver size and also by increasing driver size as shown in Table 1,2,3 &4.It is observed that crosstalk can be minimized by interconnect optimization.

CMOS 32nm Technology

TABLE I: NORMAL WIRE SIZE WITH PROPAGATION DELAY: 50NSEC

Net	R_{s1} (KΩ)	C_{c1} (pF)	C_{sub1} (e-17F)	Output (V)
Aggressor	1.12	2.97	1.2	
Victim	1.11	2.97	1.2	
Net	C_{c2} (pF)	C_{sub2} (e-19F)	R_{s2} (KΩ)	4.7
Aggressor	1.1	3.73	6.42	
Victim	1.1	3.86	6.56	

TABLE II: OPTIMIZED WIRE SPACE AND WIRE WIDTH

Net	R_{s1} (KΩ)	C_{c1} (e-19F)	C_{sub1} (e-17F)	Output (V)
Aggressor	0.01	3.76	1.2	
Victim	0.01	3.76	1.1	
Net	C_{c2} (e-19F)	C_{sub2} (e-19F)	R_{s2} (KΩ)	4.96
Aggressor	9.46	3.73	3.48	
Victim	9.46	3.86	3.40	

CMOS 55nm Technology

TABLE III: NORMAL WIRE SIZE WITH PROPAGATION DELAY: 45NS

Net	R_{s1} (Ω)	C_{c1} (e-16F)	C_{sub1} (e-15F)	Output (V)
Aggressor	45	1.299	8.464	
Victim	37	1.299	8.464	
Net	C_{c2} (e-19F)	C_{sub2} (e-15F)	R_{s2} (Ω)	4.5
Aggressor	1.28	8.4	307	
Victim	1.27	8.4	316	

TABLE IV: OPTIMIZED WIRE SPACE AND WIRE WIDTH

Net	R_{s1} (Ω)	C_{c1} (e-18F)	C_{sub1} (e-14F)	Output (V)
Aggressor	0.001	5.76	1.2	
Victim	0.001	5.76	1.2	
Net	C_{c2} (e-19F)	C_{sub2} (e-14F)	R_{s2} (Ω)	4.96
Aggressor	1.32	1.2	0.001	
Victim	1.32	1.12	0.001	

IV. CONCLUSION

In this paper, we presented a 2π crosstalk noise model which incorporates all victim and aggressor driver/ interconnect physical parameters including coupling locations on both victim and aggressor nets. We derived analytical expressions for the important metrics of crosstalk noise height and width using this model. Crosstalk noise minimization technique using on-chip wire spacing and sizing are also developed and validated for deep submicron technologies. Output voltage is observed for normal wire size as well as for optimized wire size/spacing and shown that crosstalk can be minimized by interconnects optimization.

REFERENCES

[1] S. I. Association, "The international technology roadmap for semiconductors", 1999.

[2] J. Cong, D. Zhingang, and P. V. Srinivas, "Improved crosstalk modeling for noise constrained interconnect optimization", In *Proceedings of ASP/DAC Asia South Pasific Design Automation Conference*, pp. 373–378, 2001.

[3] P. D. Gross, R. Arunachalam, K. Rajagopal and L. T. Pileggi, "Determination of worst-case aggressor alignment for delay calculation", In *Proceedings of the IEEE International Conference on Computer-Aided Design, ICCAD-98*, 1998.

[4] S. Sirichotiyakul, D. Blaauw, C. Oh, R. Levy, V. Zolotov and J. Zuo. Driver modeling alignment for worst-case delaynoise. In *Proceedings of Design Automation Conference DAC*, pp. 720–725, June 2001.

[5] S. Alwar, D. Blaauw, A. Dasgupta, A. Grinshpon, R. Levy, C. Oh, B. Orshav, S. Sirichotiyakul and V. Zolotov. Clarinet: A noise analysis tool for deep submicron design. In *Proceedings of Design Automation Conference DAC*, pp. 233–238, June 2000.

[6] K. L. Shepard and V. Narayanan, "Noise in deep submicron digital design", In *Proceedings of ICCAD-96 Intl. Conferenceon Computer Aided Design*, pp. 524–531, Nov. 1996.

[7] T. Sakurai., "Closed-form expression for interconnect delay, coupling, and crosstalk in VLSIs", *IEEE Transactions on Electron Devices*, 40:118–124, 1993

[8] A. Vittal and M. Marek-Sadowska, "Crosstalk reduction for VLSI", *IEEE Transactions on Computer Aided Design*, 16:290–298, March 1997.

[9] A. Vittal, L. H. Chen, M. Marek-Sadowska, K. P. Wang and S. Yang. "Crosstalk in VLSI interconnections", *IEEE Transactions on Computer Aided Design*, 18:1817–1824, Dec. 1999.

[10] A. B. Kahng, S. Muddu, and D. Vidhani. Noise and delay uncertainty studies for coupled rc interconnects. In *Proceedings of ASIC/SOC Conference*, pages 3–8, 1999.

[11] A. Devgan, "Efficient coupled noise estimation for on-chip interconnects", In *Proceedings of the IEEE International Conference on Computer-Aided Design, ICCAD-97*, pp. 147– 153, 1997.

[12] M. Kuhlmann and S. S. Sapatnekar. Exact and efficient crosstalk estimation. *IEEE Transactions on Computer Aided Design*, 20(7):858–866, July 2001.

[13] A. Vittal and M. Marek-Sadowska, "Crosstalk reduction for VLSI," *IEEE Trans. on Computer- Aided Design of Integrated Circuits and Systems*, Vol. 16, pp.290-98, 1997.

[14] S. Nakagawa, D. M. Sylvester, J. McBnde, and *S. Y.* Oh, "On-chip cross talk noise model for deep submicrometer ulsi interconnect," *Hewlett-Packard Journal,* vol. 49, pp. 39-45, Aug. 1998.

[15] A.B. Kahng, S. Muddu, and D. Vidhani, "Noise and delay uncertainty studies for coupled rc interconnects," in *IEEE International ASIC/SOC Conference,* pp. 3-8,1999

[16] M. Kuhlmann, *S.* Sapamekar, and K. Parhi, "Efficient crosstalk estimation," in *Proc. IEEE International Conference on Computer Design,* pp. 266-272, 1999.

[17] E. Acar, A. Odabasioglu, M. Celik, and L. Pileggi, "S2p:a stable 2-pole RC delay and coupling noise metric IC interconnects," in *Proceedings 9th Great Lakes Symposium on VLSI,* pp. 63, 1999.

[18] A. Vittal, L. Chen, M. Marek-Sadowska, K.-P. Wang and S. Yang, "Crosstalk in VLSI Interconnections" IEE*E Trans. on Computer-Aided Design of Integrated Circuits and System,* Vol. 18, No. 2.

[19] A. Devgan, "Efficient coupled noise estimation for on-chip interconnects," in *Proc. Int. Con5 on Computer Aided Design,* pp. 147-153,1997

[20] Xiaopeng Ji, Long Ge, Xiaodong Han, Zhiquan Wang, "Crosstalk Noise Analysis for Distributed Parameter High-Speed Interconnect Lines Based on the Transfer Function", 978-1-4244-1734-6/08/$25.00/ 2008 IEEE

[21] Md. Sajjad Rahaman and Masud H. Chowdhury "Crosstalk Avoidance and Error-Correction Coding for Coupled *RLC* Interconnects", 978-1-4244-3828-0/09/$25.00 ©2009 IEEE

P. V. Hunagund received his M.Sc and Ph.D from the Department of Applied Electronics, Gulbarga University, Gulbarga, in the year 1982 and 1992 respectively. He is the Senior Professor of Applied Electronics Department, Gulbarga University, Gulbarga, INDIA.

He has more than 50 research publications in national and international reputed journals, more than 155 research publications in international symposium/Conference and more than 100 research publications in national symposium/Conference. He presented many papers in India & abroad. He has guided many Ph.D and M.Phil students. He has completed three major research projects funded by A.I.C.T.E. and D.S.T. New Delhi. At present he is the Coordinator of the Non-SAP project funded by UGC, New Delhi.

A. B. Kalpana received B.E, Degree from, S.J.C.I.T, Bangalore University, In 1995, M.E, Degree from U.V.C.E, Bangalore University, Bangalore, India in 2001, pursuing Ph.D in the Department of Applied Electronics, Gulbarga University, Gulbarga, INDIA, currently she is working as Assistant Professor in the Department of Electronics and communication, Bangalore Institute of Technology, Bangalore, INDIA, her research interests include Analysis and Design of VLSI circuits and Power Electronics.