A New Approach for Mitigation of Voltage Dips on MV/LV Distribution Network

S. Sundeep, Trinath .K, Ch. Naga Koti Kumar and Dr. P. Linga Reddy

***Abstract*--This paper studies the recovery of voltage after a voltage dip due to a fault in a power network. The instant at which voltage recovery takes place is the instant of fault clearing. Here for voltage dip mitigation a new compensation technique is introduced. It consists of energy storage component, control electronics and solid state switch. It provides varies benefits such as reduction of voltage dip and increase of voltage. Finally the principle of operation of this technique has been presented and the capability has been proved by Matlab/Simulink.**

***Index terms*--**Power Q**uality, Power Network, Voltage Dip and Control Electronics.**

I. INTRODUCTION

In present days the distribution system is facing the problems mainly with voltage dips and voltage sags. The increasing use of electronics in daily activities creates problem of power quality. The term Voltage dip is defined as, a short term reduction in, or complete loss of RMS voltage Simply the meaning of voltage dip is that, the required energy is not being delivered to the load [1].

There are two main causes of voltage dips. They are, one is due to starting of large loads either on the affected site or by a consumer on the same circuit and the second one is faults on other branches of the network.

When heavy loads are started, such as large drives, their starting current can be many times to the normal running current [2]. Since the supply and the cabling of the installation are dimensioned for normal running current, but the high initial current causes a voltage drop in both the supply network and the installation. The magnitude of this effect depends on how much strong the network is, that is, how much low the impedance is at the point of common coupling (PCC) and on the impedance of the installation cabling. Voltage Dips caused by starting currents are characterised by being less deep and much longer than those caused by network faults. Typically from one to several seconds or tens of seconds.

Voltage dips have become a major concern in power quality in the past period of ten years. The cost of economical loses and inconveniences caused by voltage dips have triggered some studies and some research activities. Many experts have tried to characterise these voltage dips. The existing standard on voltage dip characterises the voltage dips in terms of magnitude and duration of the dip.

The characterisation of this standard is based on the assumption that, the faults will cause rectangular voltage dips. It is also assumed that the voltage drops to a certain low value immediately and when the fault or dip is cleared, then the voltage recovers back to its normal position immediately.

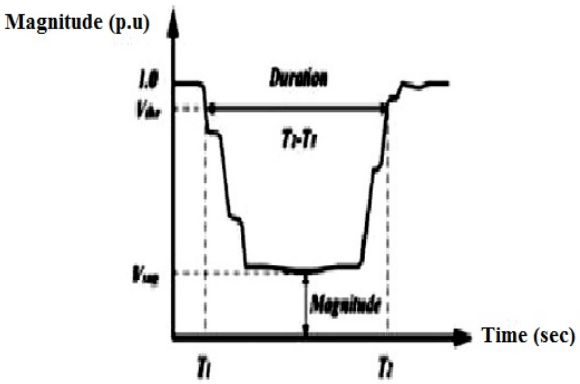

Fig 1: Voltage Dip

But it is proved that the voltage dips which occur on a system, does not have any rotating machines result in a rectangular profile dip[1]. The voltage directly drops to a particular level during fault or dip. After that when it is cleared, the voltage returns to the original level which is present before the fault or dip occurred.

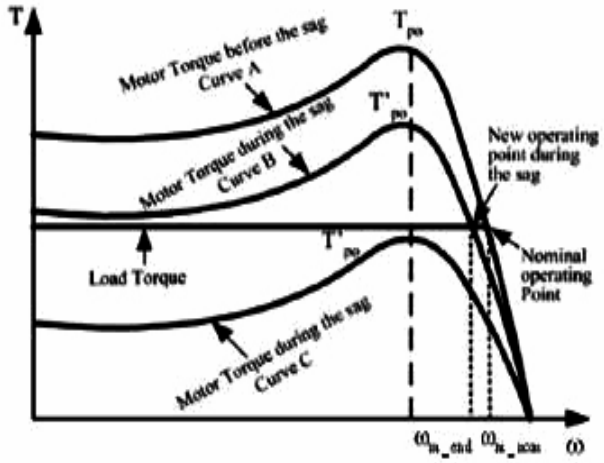

Fig 2: Motor and Load torques before and during different sags

A different phenomenon can be found in a system with rotating machine loads [2]. When a fault occurs, the voltage does not directly drop to its minimum level but it decays until reaching a steady condition before the fault is cleared. At that time, the voltage does not directly return, but recovers slowly until reaching its original level.

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S.Sundeep is with dept of Electrical and Electronics Engineering, faculty of CMR Institute of Science and Technology, Hyderabad. (E.mail: s.sundeep1@gmail.com)

As we know about the dc to ac converters, When the output currents exceed the rated values, these will function with limited current, then protection selectivity and induction motor start up cannot be guaranteed in power electrical systems fed by this dc to ac converters.

In recent trends, the dynamic voltage restorer (DVR) [5-8] has been used for the sake of protection and it installed in distribution network. When a fault occurs in a distribution network, a sudden voltage dip will occurred on adjacent load feeders. In this kind of situation if a DVR installed on the associated path, then the line voltage is restored within a short period. So the equipment, apparatus and sensitive device will not be affected.

This DVR (Dynamic voltage restorer) usually consists of harmonic filter, isolation transformer, voltage source converter, energy storage component, control electronics and solid state switch. But one of the existing problems of this DVR is the dynamic performance. It is necessary for the device to respond to the voltage dip which occurred for a few milliseconds. The energy storage components must be optimized in terms of the size, duration of the voltage dip and amount of voltage dip. The harmonic generated by the switching converter must be properly filtered. The reliability of the device is another concern. This technology cannot solve all the above shortcomings. The power density of a DVR is also a challenge [12]. The power density of DVRs is therefore poor and the material cost is high.

II. Operation With Dvr

In this operation, it has an inverter to produce the sinusoidal voltage and its amplitude is varied according to the required output voltage of the system after a voltage dip, which is followed by a fault. The usual method used to regulate the inverter's output to maintain constant output voltage in the critical devices. The below Fig 3 shows a schematic diagram for the entire operation. ZL and CB are line impedance and circuit breaker respectively. Here the energy storage device, inverter, isolation transformer and filter all together form the large components of a DVR. During the process in case if there is no fault, a Static Triac is usually used to bypass the DVR. But it can be seen that when there is a fault appeared in Load 1, the inverter is triggered to generate a sinusoidal voltage that is added in series to the bus of the load 2.

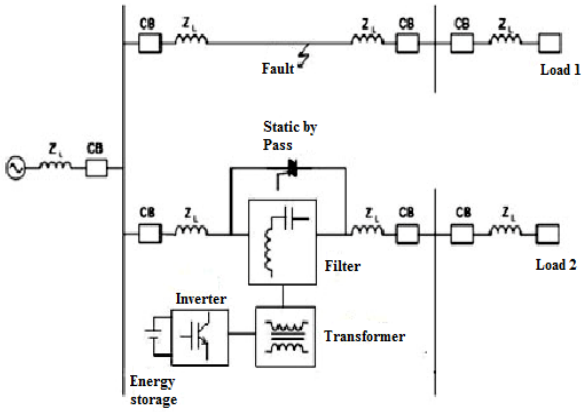

Fig 3: Schematic of a classical DVR

Generally, a transformer is used for isolation and to connect the inverter output voltage in series with the bus [10]. Here, a filter is installed to remove the pulse width modulated high frequency carrier. Fig 4 shows that the output voltage from the inverter and the voltage take a few cycles to reach the required value.

The drawback is that the voltage requires considerable time to rise to required voltage because of the delay due to the filter [9]. Another drawback of this method is that the transformer has to handle through 50Hz main frequency power. We know that as the magnetic field is inversely proportional to the operational frequency, so it is necessary to increase the transformer size in order to reduce the magnetizing magnetic field of the transformer core. Then as a result, the size of the transformer is increased and it will significantly increase the size and cost of the system.

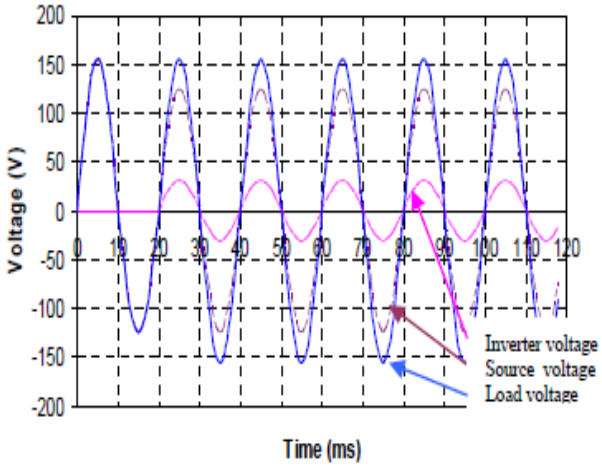

Fig 4. The voltages of the source, inverter and load under a voltage sag with the compensation of a DVR.

III. Praposing Classical Compensation

Other than the basic DVR, the recent development in power conversion also provides other methods of solution to the above problems. This includes new topologies proposed for power conversion and isolation that give alternative methods for the switching electronics [14-17]. Inductor design techniques give advanced method to design high frequency magnetic energy storage and isolation [18-20]. Switched-capacitor techniques [17-21] give the latest method for switching capacitor operation and energy storage. Power factor correction (PFC) with resonant switching gives low EMI for the improvement of power quality [19].

The general architecture of the total arrangement is shown in Fig. 5, the parameters of the Source rating, transformers rating, load rating and line rating are given in the Appendix. This considers one phase of the system. The series-connected inductors and the shunt-connected capacitors are designed in order to realize parallel resonance at the fundamental frequency. Until the control system detects a fault, the static Triac is usually used to bypass the compensation arrangement.

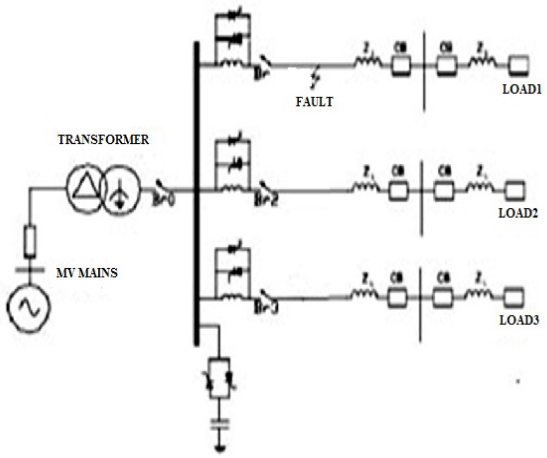

Fig 5. Schematic diagram for classical compensation

So, the energy injection arrangement is transparent to the network and does not affect the operation of the load. But when the system detects a fault appeared on a load1, the capacitor bank inject the voltage into the bus, by turning on static device which is in series with the energy storage element.

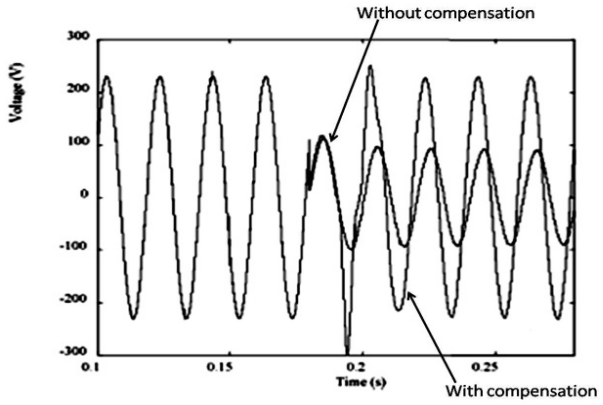

Fig 6. With and Without Compensation

The following benefits are obtained:
• Cost of operation is less.
• Size of equipment is reduced
• A mitigation of the voltage dip at the point of common coupling (PCC).
• Fast operation.
In order to study this operation, we have to identify:
• The time at which the fault occurs;
• The time at which device is to be insert;
• The fault impedance;

IV. Conclusion

In this paper, the working operation of the compensation device presented. In the case of a fault detected in a passive network, it reduces the voltage dip by increases the PCC voltage.
The following benefits are obtained:
• Cost of operation is less.
• Size of equipment is reduced
• A mitigation of the voltage dip at the point of common coupling (PCC).
• Fast operation.

Finally, the preliminary experimental results of prototype device are agreeing with the simulation results.

V. Appendix

Source rating:

1. Source phase-phase voltage is 33Kv.
2. Frequency is 50 Hz.

Transformer rating:

1. This is 33/0.44 Kv/Kv transformer.
2. Its Nominal power is 250MVA.
3. Frequency is 50Hz.

Load ratings:

Load	V_{AVG} (VOLTS)	Freq (Hz)	P (KW)	Q (KVAR)
L_1	440	50	35	1
L_2	440	50	15	1
L_3	440	50	20	1

Line ratings:

Line Name	Length(Km)
TL1	**30**
TL2	**10**
TL3	**10**

References

[1]. M.F. McGranaghan, D.R. Mueller, and M.J. Samotyj, 'Voltage Sags in Industrial Systems", IEEE Transaction on Industry Applications, Vol. 29, No. 2, pp. 397-403, April 1993.
[2]. J.C Das, The effects of momentary voltage dips on the operation of induction and synchronous motors, IEEE Trans. Ind. Applicat., vol.26, pp.711-718, 1990.
[3]. P. G. Slade, J. L. Wu, E. J. Stacey, W. F. Stubler, R. E. Voshall, J. J. Bonk, J. W. Porter, and L. Hong, "The utility requirements for a distribution fault current limiter," *IEEE Trans. Power Del.*, vol. 7, no. 2, pp. 507–515, Apr. 1992.
[4]. G. Yaleinkaya, M. H. J. Bollen, and P. A. Crossley, "Characterization of voltage sags in industrial distribution systems," *IEEE Trans. Ind. Appl.*, vol. 34, no. 4, pp. 682–688, Jul./Aug. 1998.
[5]. H.D.T.Mouton, and A.J.Visser, "250kW transformer-less voltage dip compensator", IEEE AFRICON, 1999, Vol 2, pp. 865-870.
[6]. M.Barnes,N.Jenkins, C.Zhan and V.K.Ramachandaramurthy "Dynamic voltage restorer with battery energy storage for voltage dip mitigation", IEE Power Electronics and Variable Speed Drives, 2000, pp. 360-365.
[7]. H.Foch, P.Michalak, H.Pouliquen and R.Tounsi, "Control laws for a voltage dip series compensator", IEE Power Electronics and Variable Speed Drives, 2000, pp.21-23.
[8]. D.Armhof, P.Dahler, H.Gruning and A.Kara, "Power supply quality improvement with a dynamic voltage restorer", APEC, 1998, vol. 2, pp. 986-993.
[9]. C.Fitzer, M.Barnes and P.Green, "Voltage sag detection techniques for a dynamic voltage restorer", IEEE Transactions on Industry Applications, Vol. 40, No. 1, January 2004, pp. 203-212.
[10]. K.W.E.Cheng, "Zero-voltage-switching modulation technique for resonant pole inverter", IEE Electronics Letters, April 1999, Vol. 35, No. 9, pp. 692-693.
[11]. Y.Kataoka, K.Matsushita, M.Ono, " High speed switchgear protecting power generating facilities against voltage dip and interruption", Power Electronics and Drive Systems 1995, vol. 2, pp. 726-731.

[12]. Y.P.B.Yeung, K.W.E.Cheng, S.L.Ho and D.Sutanto, "Generalised analysis of switched-capacitor step-down quasi-resonant converter", IEE Electronics Letters, Vol 38, Issue 6, March 2002, pp. 263-264.
[13]. S.Y.R.Hui, K.W.E.Cheng and S.R.N.Prakash, `A fully soft-switched extended-period quasi-resonant power-factor-correction circuits', IEEE Transactions on Power Electronics Vol. 12, No. 5, Sep 1997. pp. 922- 930.
[14]. K.W.E.Cheng and P.D.Evans, 'The unified theory of extendedperio quasi-resonant converter', IEE Proceedings-Electr. Power Appl., Vol. 147, No. 2, March 2000, pp. 127-132.
[15]. K.W.E.Cheng, "Zero-voltage-switching modulation technique for resonant pole inverter", IEE Electronics Letters, April 1999, Vol. 35, No. 9, pp. 692-693.
[16]. Y.P.Yeung, K.W.E.Cheng, D.Sutanto, and S.L.Ho, "Zero-current switching switched-capacitor quasi-resonant step-down converter", IEE Proceedings – Electr. Power Appli., Vol 149, Issue 02, March 2002, pp. 111-121.
[17]. Y.P.B.Yeung, K.W.E.Cheng, S.L.Ho and D.Sutanto, "Generalised analysis of switched-capacitor step-down quasi-resonant converter", IEE Electronics Letters, Vol 38, Issue 6, March 2002, pp. 263-264.
[18]. K.W.E.Cheng and P.D.Evans, 'Calculation of winding losses in high frequency toroidal inductors using single strand conductors', IEE Proceedings-Electr. Power Appl., Vol. 141, No. 2, March 1994, pp. 52-62.
[19]. K.W.E.Cheng and P.D.Evans, 'Calculation of winding losses in high frequency toroidal inductors using multi-strand conductors', IEE Proceedings-Electr. Power Appl., Vol. 142, No. 5, September 1995, pp. 313-322.
[20]. K.W.E.Cheng, "Computation of the AC Resistance of Multistranded Conductor Inductors with Multilayers for High Frequency Switching Converters", IEEE Transactions on Magnetics, Vol. 36, No. 4, July 2000, pp. 831-834.
[21]. Y.P.Yeung, K.W.E.Cheng and D.Sutanto, "Investigation of multiple output operation for switched-capacitor resonant converters", Int.J. Cct Theory&App, Vol. 30, Issue 4, Mar 2002, pp. 411-423.

Sundeep.S, was born 1987. He received his B.Tech in Electrical Engineering from JNTU Hyderabad and M.Tech in Power Electronics and Power Systems from K.L University Vijayawada. Currently he is working as Asst. professor in CMR Institute of Science and Technology, Hyderabad. His area of interests is power systems and power Quality.

Trinath.K was born 1987. He received the B.Tech in Electrical Engineering from JNTU Kakinada & M.Tech in Power Electronics & Power Systems from K.L University Vijayawada. His area of interests is power systems.

Ch. Naga Koti Kumar was born 1987. He received the B.Tech in Electrical Engineering from JNTU Kakinada & M.Tech in Power Electronics and Power Systems from K.L University Vijayawada. His area of interests are power systems and Electrical Motors controlling.

Dr.P.Lingareddy was born in 1939.He received his PhD from I.I.T (Delhi).He has a teaching experience of 42 years. Currently he is professor in school of electrical and electronic engineering K L University Guntur. He has many publications in the area of control systems. His area of interests are power systems and control systems.

from left to right. In Gurmukhi, there is no concept of upper or lowercase characters. There are 41 consonants and 12 vowels in Gurmukhi script alphabet. These are shown in Figure 2 (a) and (b).

Fig. 2. a) Gurmukhi Consonants

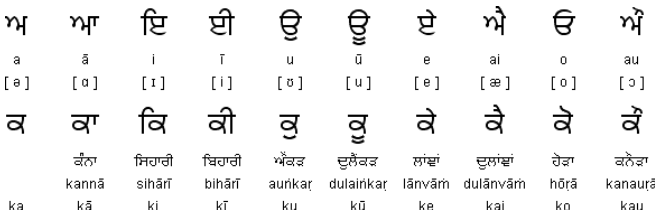

Fig. 2. b) Vowels and diacritics (Laga Matra)

The Gurmukhi script is a two dimensional composition of consonants, vowels and half characters which require segmentation in a vertical as well in horizontal direction. Thus the segmentation of Gurmukhi text calls for a two dimensional analysis instead of commonly used One dimensional analysis for Roman script.

III. Preprocessing

It is a process of representing the scanned image for further processing. The raw data, depending on the data acquisition type, is subjected to a number of preliminary processing steps to make it usable in the descriptive stages of character analysis. Pre processing aims to produce data that are easy for the CR systems to operate accurately. Preprocessing is applied on the input binary document so that the effect of spurious noise can be minimized in the subsequent processing stages. It is supposed that height and width of document can be known easily. The image file is in grey scale. But we require two types of information either zero or one. For that purpose, we calculated the average of intensities of all the pixels present in the document image file. Then the intensity of each pixel is set as per the following rule:

if (pixel intensity < Average intensity) then pixel intensity = 0 else pixel intensity = 1

Scan every pixel of document and compare its intensity with the maximum intensity. If the intensity is equal to maximum intensity, store one in the array at that location, and if it is not equal store zero in the array. The quality of scanned image depends upon the scanner type too and it plays an important role in segmentation. We are using higher end scanner for the scanning purposes. But even if some impurities are introduced due to used paper quality or due to scanner quality then these are taken care by using anti windowing concept. As per this concept, first the area is searched with a window of width dw. If there is only few pixel and nothing is around the window then those intensities of present pixel values are set to zero. The words and characters are handwritten. Between any two lines and any two words there is a definite gap of minimum width. A line is supposed to have different words and the words are made up of one or more characters. The lines consisting of words are generally straight in nature. If there is any skew then present work may not work properly.

IV. Algorithm to Segment Line, Word and Character

Get the window coordinates. A pixel position is defined as a point which is taken as POINT { Int X;Int Y;}. For whole of the window, find areas of no pixel zones, store to some file. For two consecutive no pixel zones – find the minimum and maximum of X coordinates and find the minimum and maximum of Y coordinates. Write the min and max of X and Y in a file. The formal algorithm is given below:

Procedure to find Lines

- Read the Initial values of BMP, it will give the starting point of the file and the size of file. (// this will enable us to find starting and ending point of BMP file, having the handwritten image .)
- LOC = Starting Point of the image
- Do while (Not end of Input file)
  - Call Boundary_ Vertical (LOC as POINT, d as integer, X as integer, MaxY as integer, MinY as integer)
  - Call Horizontal Boundary (LOC as POINT, MaxY as integer, MaxX as integer, MinX as integer)
  - Write in OFILE, MinX,MinY, MinX, MaxY, MaxX, MaxY, MaxX, MinY
  - LOC.x = MinX and LOC.Y = MinY

  End of While

Procedure to find Words

- From the data file, get window coordinates of first two lines store to L1 and L2.
- While (L1 or L2 < > NULL)
  - Check the distance between the windows of L1 and L2. If it is less than a predefined value then merge these two windows of L1 and L2 to one large window (say) L1 and write the coordinates of L1 to the file and replacing L2.
  - If L2 is replaced then Set L2 = next line from file.
  - Set L1= L2 and L2 = next line from file
- End While
- Do while (Not All Lines are processed)
  - L = Get the Line from Input file
  - LOC.X=MinX of line L and LOC.Y = MinY of Line L
  - Do while (Not end of Window of L)
    - Call Boundary_Vertical(LOC, d, Y as integer, MaxX as integer, MinX as Integer)