Fast Adder Design using Redundant Binary Numbers with Reduced Chip Complexity

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Abstract—**Redundant Binary Signed Digit Adder and Multiplier circuits are logic circuits which are designed to perform high-speed arithmetic operations. Fast RBSD adder cell, proposed by Kal and Rajshekhar in 1990 was modified by Neelam Sharma in 2006 using universal logic. The proposed adder is re-modified for reducing the number of gates and thus the circuit complexity and cost. Further due to the reduced gate count, circuit area, number of levels and hence implementation time is reduced up to 1% as proved by VHDL synthesis report. Since multiplication is repetitive addition, the implementation time of the multiplier circuit will be reduced to a great extent. Thus the proposed RBSD adder cell using NOR and NAND gates will be a boost in the speed of sophisticated ALU Design of high speed machines.**

Index Terms—**Carry free addition, fast Multiplier, Fast Computing, High-speed arithmetic, RBSD.**

I. INTRODUCTION

Addition is the basic arithmetic operation for all mathematical operations like multiplication, division, square rooting etc. With recent development in technology of integrated circuits, various high-speed circuits with regular structures and low power design have been proposed. The circuits for arithmetic operations still suffers some problems like propagation time delay, limited range of the number of bits and complexity in hardware. Redundant Binary Signed Digit (RBSD) numbers is particularly gaining much attention due to the capability of carry free addition [1], [2], [3].

The performance of circuit also depends upon the suitable hardware design. The logic gates are responsible for the high-speed arithmetic operations [4]. Therefore it is highly desirable to construct digital logic circuits using universal gates because of simplicity and uniformity in circuit. These circuits just have a single primitive component of universal gate i.e. either NOR or NAND gate. Since these gates can be manufactured quite economically, therefore they contribute to the major components used today by logic designers. The use of field programmable gate arrays (FPGA) allows the development of high performance customized hardware. Selecting suitable arithmetic algorithms and applying optimal mapping strategies for FPGA technology can develop the high performance implementations [5].

This paper emphasizes briefly about RBSD number system and RBSD adder design in the sections 2 and 3. The concept of logic design for RBSD adder cell suggested by Kal and Rajshekhar in 1990 [6] and by N. Sharma et. al. in 2006 [7] is described in the sections 4 & 5 respectively. Further in section 6 the modified architecture of adder cell using universal logic has been proposed. The comparison among the previous and proposed cell structures is given in section 7. Finally in section 8, comparison among Ripple carry adder (RCA), Carry Look Ahead adder (CLA) and RBSD adder upto 64 bit length is presented.

II. REDUNDANT SIGNED DIGIT NUMBER SYSTEM

This number system was proposed by Avizienis in 1961 [1]. RBSD numbers can be represented using the digit set (1, 0, $\bar{1}$) unlike binary number system, which is represented, with digit set (0, 1). The decimal value of RBSD number can be calculated by following relation.

$$D = \sum_{i=0}^{n-1} x_i 2^i \tag{1}$$

Let the number $(4)_{10}$ can be represented in binary as 0100. The same number in RBSD may be represented by more than one representation i.e. 1 $\bar{1}$00 or 1 $\bar{1}$ $\bar{1}$00. Hence in this number system, a number can be represented by more than one way, called redundant representation. This redundant number representation proceeds to the technique for carry free addition [2].

III. ADDER DESIGN

Adder is the basic building block for the computation of all mathematical operations. Hence a carry free adder design is highly desirable when the number of bits becomes large. It can be achieved with the help of RBSD number system [9], [10], [11].

The following equations suggested by Rajshekhar and Kal, are used for the carry-free addition [6].

$$x_i + y_i = 2 * t'_{i+1} + w'_i \tag{1}$$

$$w'_i + t'_i = 2 * t''_{i+1} + w''_i \tag{2}$$

$$s_i = w''_i + t''_i \tag{3}$$

Where $|t'_i| = 1$ only if $|x_i' + y_i'| >= 1$
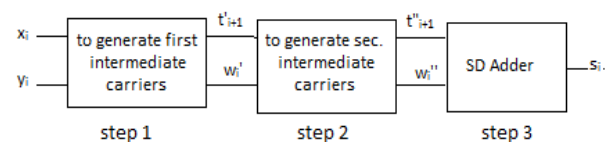and $|t''_{i+1}| = 1$ only if $|w_i' + t_i'| = 2$. $\tag{4}$

Fig. 1. Three step RBSD Addition Process

The three step RBSD addition process described by equations 2-4 is shown in fig. 1 in which first and second step generates intermediate carriers (carry and sum) and third step gives the final result. The variables x_i, y_i are the addend and augends in RBSD, t_i' and t_i'' are intermediate carriers, w_i' and w_i'' are the intermediate sums at the ith stage, 's_i' is the final sum. The variables t_i'' and w_i'' can never be both $+1$ and -1 simultaneously at second stage and hence gives carry free addition. Therefore the input numbers can be added simultaneously in parallel, as there is no rippling of carry from LSB to MSB.

IV. RBSD ADDER CELL

It is known that the logic gates do not support the negative logic (-1) therefore to represent -1, 0, 1 in RBSD the binary encoded form i.e. (0, 1), (0, 0), (1, 0) is used to encode -1, 0, 1 respectively. With this idea, Kal and Rajashekhar, 1990 has given following Boolean expressions (equation 5 to 9) for RBSD addition in binary encoded form [6], [7].

$$d_i = m_i \oplus \overline{x_i^+}\ \overline{x_i^-} \oplus \overline{y_i^+}\ \overline{y_i^-} \tag{5}$$

$$m_{i+1} = \overline{x_i}^+\ \overline{y_i}^+ \tag{6}$$

$$b_{i+1} = \overline{m_i}\ \overline{x_i^+}\ \overline{x_i^-} + \overline{x_i^+ y_i^+} + \overline{y_i}^+\ \overline{y_i^-}\ \overline{m_i}$$
$$+\ \overline{x_i^+}\ \overline{x_i^-}\ \underline{\overline{y_i}^+}\ \overline{y_i^-} \tag{7}$$

$$s_i^+ = \overline{d_i}\ \underline{b_i} \tag{8}$$

$$s_i^- = d_i\ \overline{b_i} \tag{9}$$

where m_i, b_i and d_i are binary variables and x_i^*, y_i^* are RBSD input numbers and s_i^* output sum in RBSD with digit set (-1, 0, 1) represented by binary encoded form i.e. (0, 1), (0, 0), (1, 0) respectively. The binary variable representation corresponding to augends' (x_i^*), addend (y_i^*) and sum (s_i^*) are $x_i^+ x_i^-$, $y_i^+ y_i^-$ and $s_i^+ s_i^-$ respectively.

TABLE 1: VARIABLE USED

x_i^+	xip
x_i^-	xin
y_i^+	yip
y_i^-	yin
m_i	mibar
m_{i+1}	mi_n
$\overline{m_{i+1}}$	mibar_n
$\overline{b_i}$	bibar
b_{i+1}	bi_n
$\overline{b_{i+1}}$	bibar_n

The circuit shown in fig. 2 is the RBSD adder cell implemented using equations 5-9 and suggested by Kal et.al.

This cell designed to add 1 bit RBSD number. The same circuit connected in parallel can be used to add n bit numbers. In this logic diagram, the various inputs and outputs used from the equations 5-9 which are expressed as per table 1 and are further used for the simulation of RBSD adder cell using universal logic.

V. RBSD ADDER CELL USING UNIVERSAL LOGIC

In 2006, N Sharma et. al. proposed the adder cells using universal logic [7]. The logic circuit design using universal gates is highly desirable due to uniformity in the circuit. These circuits can be designed through either NOR or NAND gates as these gates are in-expensive in manufacturing aspects, therefore they are preferred by the logic designers.

Universal gates are available in SSI package that vary in size containing up to four gates per package. Keeping above aspects in mind the adder cell shown in figure 2 is redesigned using NOR-NOR logic and NAND-NAND logic as shown in figure 3 and 4 respectively.

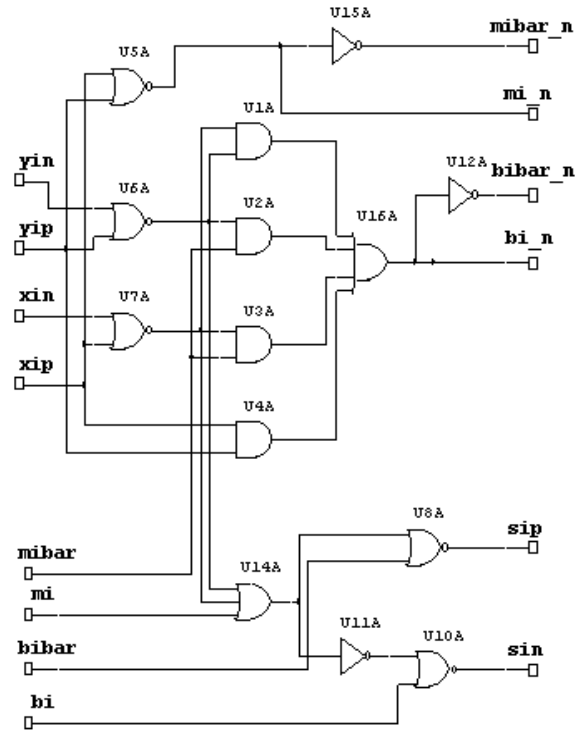The delay time of these adder cells found less as compared to the previous circuit suggested by Kal [7].
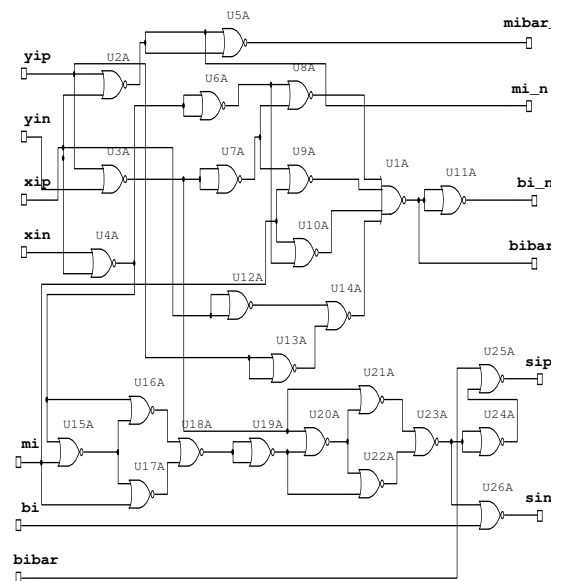

Fig. 2. Logic circuit of Basic RBSD adder cell

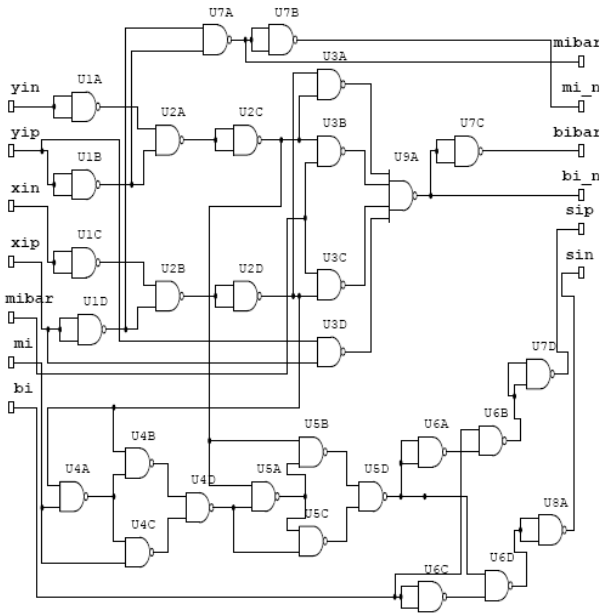Fig. 3. RBSD Adder Cell: NOR-NOR Logic

Fig. 4. RBSD Adder Cell: NAND-NAND Logic.

VI. MODIFIED RBSD ADDER CELL DESIGN USING UNIVERSAL LOGIC

In this section, the modified architectures of adder cell with reduced number of (i) NOR gates and (ii) NAND gates has been proposed as compared to the design shown in figure 3 and 4.

A. Methodology to reduce the Gate count

The reduction in gate count in proposed designs is basically due to the redesign of three input XOR gate (used in fig. 2) with universal logic.

The basic logic equation for 3-input XOR gate shown in fig. 5(a) is

$$Y = A \oplus B \oplus C \quad \text{(Let A, B, C input and Y output)}$$
$$= \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + ABC \quad (10)$$

The above logic equation can be implemented using 4 AND and 1 OR gate as shown in figure 5(b).

This logic diagram can also be implemented using 6 NOR gates or 5 NAND gates shown in figure 5(c) and 5(d) respectively by replacing equivalent universal logic implementation of 3 input AND and 4 input OR gate used in fig. 5(b) and on applying changed inputs (i.e. A B $\overline{C}$, A $\overline{B}$ C, $\overline{A}$ B $\overline{C}$, $\overline{A}$ $\overline{B}$ $\overline{C}$) to the various 3-input NOR gates.

B. Modified Adder Cell

The output d_i produced by 3-input XOR gate in basic RBSD adder cell (refer fig. 2) has been achieved after 10 NOR gates (U15A to U24A) in the adder cell proposed by N Sharma using NOR-NOR logic as shown in figure 3. In other words here the 3 input XOR logic was prepared using 10 NOR gates and passing the signal over 8 logic levels. But in proposed modified design the same output can be achieved using 6 NOR gates (U5A, U11A, U15A, U16A, U18A and U19A) only and 3 logic levels as shown in fig 6. Hence the Modified adder cell has been designed using 22 NOR gates only.

Similarly the output d_i in NAND-NAND adder cell proposed by N Sharma shown in fig. 4 has been achieved after 8 NAND gates (U4A, U4B, U4C, U4D, U5A, U5B,

U5C & U5D) and passing the signal over 7 logic levels. But in proposed modified design the same output can be achieved using five NAND gates (U7A, U7B, U7C, U8A & U6B) only and after 2 logic levels as shown in fig 7. One more NAND gate is reduced due to no need of signal mi_n for further stages in modified design. Hence the Modified adder cell has been designed using 26 NAND gates only.

It is clear from the figure 6 and 7 that the increased performance of these circuits in comparison to the circuit shown in fig 3 and 4 is due to decrement in the count of NOR gates and NAND gates which cause reduction in circuit area. Further the reduction in logic levels to travel the signal causes reduction in the propagation delay time to get the output.
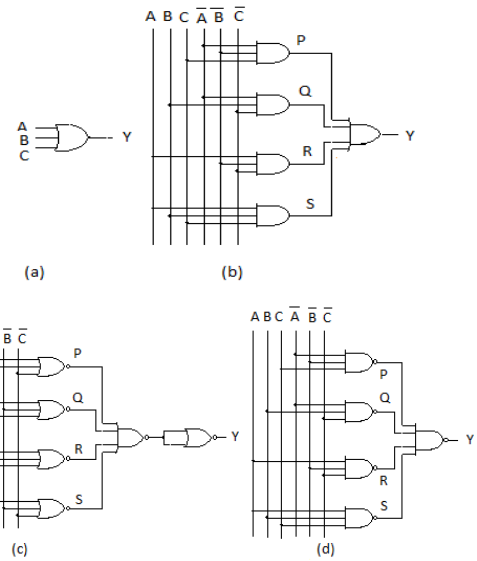

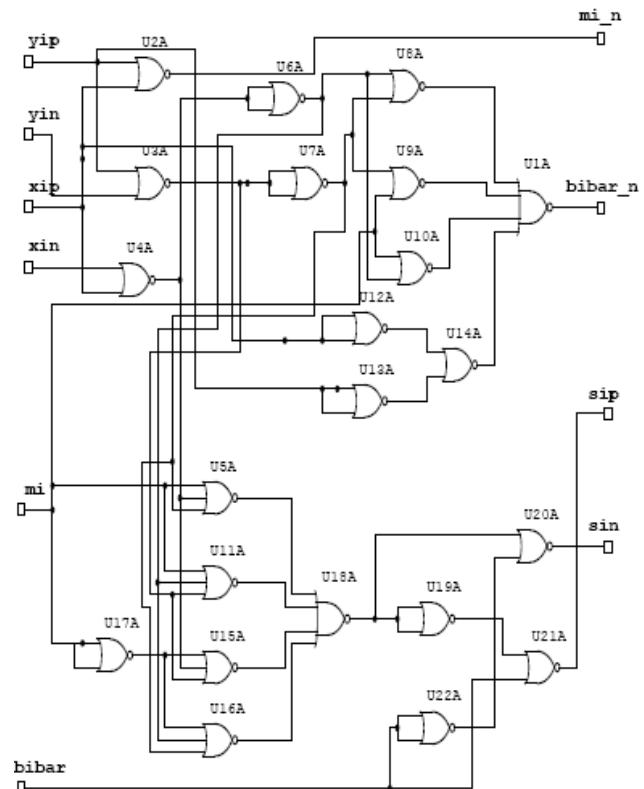Fig. 5. (a) 3 input XOR (b) 3 input XOR using AND & OR gates (c) using NOR gate (d) using NAND gate

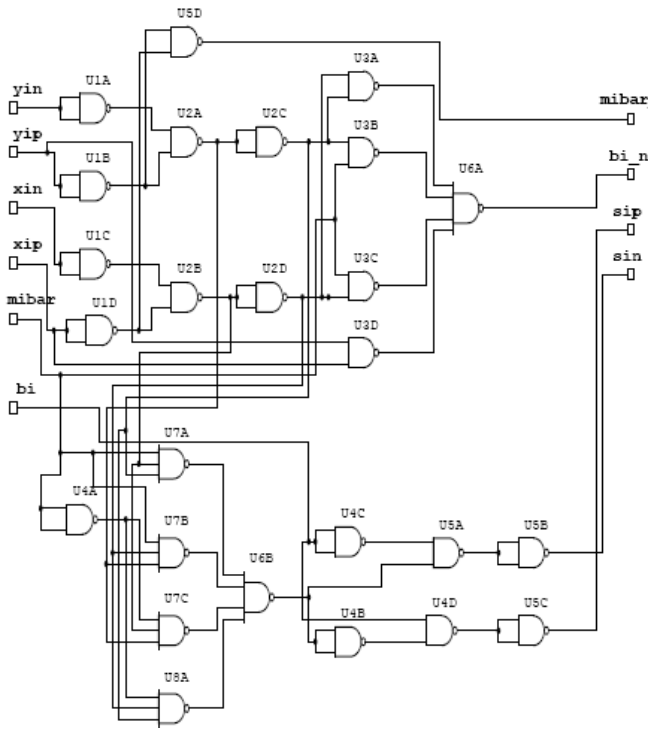
Fig. 6. Modified Cell: NOR-NOR logic

Fig. 7. Modified Cell: NAND-NAND logic

VII. COMPARISON OF VARIOUS ADDER CELL

A. Hardware

Table 2 shows a clear comparison among the circuit shown in figure 3, 4, 6 and 7. It is clear that the proposed modified architectures are better due to less number of gates required, less number of input pins and signal passes less number of levels to get the final sum.

TABLE 2: COMPARATIVE ANALYSIS AMONG VARIOUS ADDER CELLS

Type of Adder Cell	NOR / NAND Gate used				I/P Pins	Levels Required for O/P	
	2 I/P	3 I/P	4 I/P	Total		s_i^+	s_i^-
NOR-NOR	25	--	1	26	7	9	8
Modified NOR-NOR	16	4	2	22	6	6	6
NAND-NAND	29	--	1	30	7	11	10
Modified NAND-NAND	20	4	2	26	6	8	8

B. Simulation

All the adder cell architectures are verified using Multisim software. Further the VHDL code is also generated on Xilinx project navigator for the simulation, synthesis and the timing reports generation. These circuits are also verified on field programmable gate arrays (FPGA).

C. Time Delay

The propagation delay time reports using Xilinx Project Navigator (Software for VHDL synthesis) were generated and results obtained are shown in table 3 and in fig 8. Here it can be concluded that the delay time to get the addition result for one bit addition is less and reduced up to 1% in modified architectures as compared to previous one.

TABLE 3: TIME DELAY

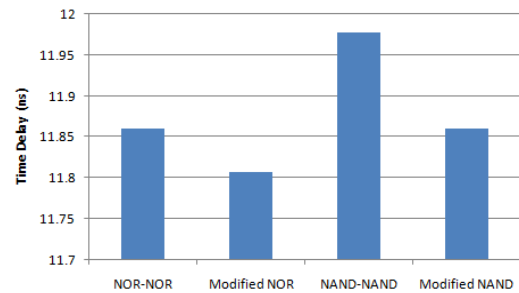| RBSD Adder Cell Type	Time Delay (ns)	Percentage (%) Reduction in Time Delay
NOR-NOR	11.861	--
Modified NOR-NOR	11.807	0.455 (Compared to NOR -NOR Logic)
NAND-NAND	11.978	--
Modified NAND-NAND	11.861	0.9767 (Compared to NAND-NAND Logic)

Fig. 8. Time delay in different architectures of Adder cell

VIII. IMPLEMENTATION AND TIMING ANALYSIS OF RCA, CLA AND RBSD ADDER

In this section the VHDL implementations of Ripple carry adder (RCA), Carry Look Ahead Adder (CLA) [12] and RBSD adder of n-bit is simulated on modelsim simulator and synthesized on xilinx project navigator and their timing reports were observed.

A comparative graph among RCA, CLA and RBSD adder is shown in figure 9. It is observed that the delay produced in RBSD adder is constant (16.51 ns) which is very less for any number of bit additions as compared to CLA and RCA. The addition time increases in RCA with increase in number of bits due to rippling of carry from LSB to MSB. In CLA the add time increases gradually due to logic for carry calculation and hence circuit changes with increase in bits. Hence for higher bit length, RBSD adders are suitable due to carry free addition and symmetrical circuit.
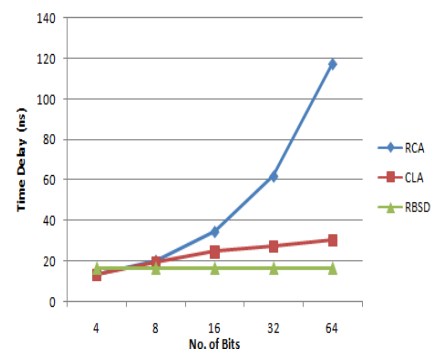

Fig. 9. Timing comparison among RCA, CLA and RBSD Adder

IX. CONCLUSIONS

The delay time of the adder cell has been reduced in the modified architectures using NOR-NOR logic and NAND-NAND logic. Hence the processing time of the basic arithmetic operations like multiplication, division, square rooting etc. can be reduced greatly. Consequently this will

improve the overall processing time of entire ALU. The number of gate counts have been reduced in the proposed adder cell from 26 to 22 in NOR-NOR and 30 to 26 in NAND-NAND logic and hence overall reduction in number of logic levels and inputs will also reduce the area and chip complexity. Therefore the proposed modified RBSD adder cell is highly appreciable for design of ALU of higher bit length.

In digital design techniques, much attention has to be paid to network design in the form of repeated pattern of identical circuits. Therefore the redundant adder has a high advantage of constant and less delay time for any number of bit additions. The CLA adders are suitable only upto 12 bit addition and thereafter addition using redundant adders is suitable for 64, 128, 256 bit adders.

The efficiency of RBSD adder increases as bit length of the summands increases. The higher the bit length, the efficiency of RBSD adder as compared to CLA will increase. Finally addition is the base for all the mathematical operations, fast arithmetic processor of higher bit length can be designed using proposed architectures of adder cell.

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