ISSN: 1793-8236

Analysis of the Effects of the Operating Temperature at the Performance and Leakage Power Consumption in a Conventional CMOS 6T-SRAM Bit-Cell at 65nm, 45nm, and 32nm Technologies

Neeraj Kr. Shukla[1], Shilpi Birla[2], R.K. Singh[3] and Manisha Pattanaik[4]

***Abstract*—For mobile and multimedia applications of SRAMs, there is a strong need to reduce standby current leakages while keeping the memory cell data unchanged. To meet this objective, various techniques have been developed to reduce the leakage current at the process/device, circuit, architecture, and algorithmic levels. The traditional 6T CMOS SRAMs face many challenges in deep-submicron (DSM) technologies for low supply voltage (VDD) operation. Predictions suggests that process variations will limit standard 90nm SRAMs to around 0.7V operation because of the Static Noise Margin (SNM) degradation and write margin, also a VDD of 0.7V is reported for a 65nm SRAM. This work discusses some of the schemes that minimizes the cell leakage regardless of the process fluctuations and the environmental conditions. Various SRAM leakage currents identifies the suitable schemes for 6T SRAM sub-threshold operation at device and circuit levels for optimal sub-threshold circuit designs and provides an effective roadmap for digital circuit designers who are interested to work with ultra-low-power applications in CMOS technology.**

***Index Terms*—DSM (Deep Sub-Micron), Power Gating, SNM (Static Noise Margin), Sub-threshold Operation, Data Retention.**

I. Introduction

Rising demand for multimedia rich applications like portable and handheld devices have tremendously increases the need for large and high performance memories like the Static Random Access Memory (SRAM). The on-die cache memory occupies a large portion of the silicon area, i.e., of the total chip area. It also plays a significant role in overall power consumption of the multimedia application. Due to continuously scaling of the CMOS devices, it is possible to have a high packaging density which helps in reducing the overall Si area. To minimize the overall power consumption, the first design factor loved by the designer community is the supply voltage (V_{DD}) reduction. This reduction in V_{DD}, though appreciates the power consumption, results in two important concerns, the data stability and the leakage power. The leakage current composes nearly 40% of total power consumption in today's high performance chip. There are several leakage reduction techniques has been introduced by the researcher community but each has to be checked and verified according to the circuit techniques and target technology without loosing the concerns in data stability, delay, etc.

This paper provides an analytical and comparative roadmap to explains which are the main components of leakage currents, and how they can be minimized using various device and circuit techniques. These techniques incorporate various biasing schemes and other methodologies that depend on the number of transistor in the CMOS SRAM Cells.

II. Sram Cell Leakage Mechanism

Fig.1 shows schematically the significant parametric cell leakage paths and mechanisms operating in the 6T SRAM. For each leakage mechanism and resolving the leakage to the given cell dimensions, the total cell and/or array leakage can be calculated effectively and the expected array leakage can be estimated adequately. In Fig.1, for the arbitrary state selected, the internal node on the left side of the latch is maintained at ground while the node on the right is held at V_{DD} by the operation of the cross-coupled latch. The intent of this section is to describe in brie the critical parametric leakage sources within the cell, derived from this latched configuration that corresponds to memory array standby mode. Although the schematic in Fig. 3 shows the gate-leakage to substrate for transistor T3 and to the n-well for T6, it needs be pointed out that the majority of the carriers are swept to the source nodes by the applied field.

In this paper, we review the critical parametric leakage mechanisms operating within the SRAM cell and describe how the mechanism was addressed in the described Ultra Low Power (ULP) technology. Five dominant parametric mechanisms to be addressed are threshold voltage optimization, gate tunneling leakage, sub-threshold leakage, reverse-bias diffusion leakage, and gate-induced drain (GIDL) leakage. Of all these mechanisms, mostly development efforts were addressed threshold voltage optimization and GIDL reduction. Some of the major leakage currents that play an important role in the power consumption of the chip are being discussed here.

IACSIT
International Association of Computer Science and Information Technology
WWW.IACSIT.ORG

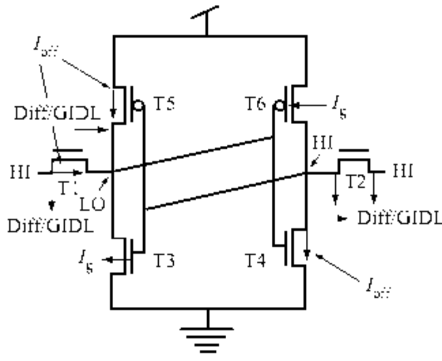


Fig.1. SRAM Leakage Current Mechanisms

(i). Gate Leakage Current

The gate tunneling leakage mechanism is active for the n-FET (T3) and p-FET (T6) sites shown in Fig 1. For the purpose described in this paper, the leakage is generally found to be adequately modeled for a given voltage as a function of gate-oxide thickness from the empirical relationship [5], for both the n-FETs and p-FETs.

$$I_g(t_{ox}) = A_0 \exp(-B_0 t_{ox})$$

Eq. (1)

Because this mechanism is governed by quantum-mechanical tunneling, this mechanism is virtually temperature-independent while other leakage mechanisms dominate at higher temperatures. This mechanism was found to establish the minimum gate-oxide thickness for the technology on the basis of the established lower-temperature leakage targets.

(ii). Vt and Sub-threshold Leakage Current

For the narrow-width devices used in the SRAM cell, the off-current of the device is elevated compared with that of a wide device because of the narrow-channel effect (NCE). The effective reduction in V_{th} associated with geometric constraints of the narrow channel is a significant challenge for future Ultra Low-Power (ULP) technologies. In the example shown, the I_{source} at zero gate bias is below 10 fA/µm at room temperature and below 600 fA/µm at 85°C for both n-FET and p-FET devices. At 25°C, it is clear that the drain current at room temperature is dominated by Gate Induced Drain Leakage (GIDL). Unlike gate-oxide tunneling leakage, sub-threshold device off-current leakage is strongly temperature-dependent and is typically the dominant leakage mechanism at higher temperatures.

Fig.1 shows the three transistors in which this mechanism is actively contributing to the standby leakage when the SRAM array is in the standby state. In the example given in Fig. 2, the internal node transistors T4 (n-FET) and T5 (p-FET) and the wordline transistor T1 (n-FET) are being held in the off state and have a drain-to-source voltage of V_{DD}. Since it is the most common for the bitlines to be held high (at V_{DD}) in standby mode, this is the mode shown for the sake of discussion. However, it is worth pointing out that if the bitlines were held low (at ground), there would still be three devices in the cell contributing to the off-state leakage, since the internal nodes of the SRAM cell are held in opposite states. The off-state leakage can be adequately characterized given the subthreshold slope parameter (B1), an extracted parameter (A1) and threshold voltage (Vt) for both the n-FET and the p-FET with the following relationship [5].

$$I_{off}(V_t, T) = C(T) A_1 \exp(B_1 V_t),$$

Eq. (2)

Where, C(T) is expressed as,

$$C(T) = 10^{(V_t/S) - [V_t - (T-298)\gamma/(T/298)S]}$$

Eq. (3)

Where, S is the sub-threshold slope, Υ is the slope of the V_{th} as a function of temperature, and T is the temperature in degrees Kelvin.

Because of the obvious importance of Vtcontrol for both array leakage and cell stability, two additional topics which relate to V_{th} control must be addressed for ULP technologies. These include the effect of device width on Vt, referred to as Narrow-Channel Effect (NCE) [15,16] and the treatment of statistical variations in V_{th} in narrow devices]. Both of these factors become increasingly important for the 0.13µm node and below. While this explanation is generally accepted for the n-FET. So far, no complete explanation has been proposed for the observed NCE in the ULP p-FET device. The observed p-FET behavior appears to be unique to the ULP technologies. As for the high-performance devices the p-FET NCE typically results in a slightly higher Vt with narrower channels. As a result of this phenomenon, the threshold voltages must be set higher than one might assume on the basis of the measured wide device off-current in order to achieve the cell leakage targets. It is well known that the statistical variation in V_{th} will become an increasing concern as devices continue to scale [18,19]. This is due to not only to the physical dimension tolerances but also to statistical variations in channel dopant associated with the reduction in channel area. This variation can be compounded in the SRAM cell by V_{th} variations associated with overlay tolerances and corner- rounding effects due to aggressive scaling to achieve maximum density for the cell. Because of the exponential relationship of I_{off} with V_{th}, the contribution of the devices in the array with lower threshold voltage must be accounted for in calculating the overall array leakage [5,7].

The array leakage increase associated with the variation in the standard deviation of V_{th}, i.e., (V_{th}), can be estimated by means of the following equation [5],

$$I_{ddx}[V_{td}, \sigma(V_t)] = \frac{\int_{V_{t1}}^{V_{t2}} \frac{1}{\sqrt{2\pi}\sigma(V_t)} e^{\{[-1/2\sigma(V_t)^2](V_{td}-\bar{V}_t)^2\}} [A_1 e^{(-B_1 V_{td})}] \, dV_{td}}{A_1 e^{(-B_1 \bar{V}_t)}},$$

Eq. (4)

Where, $\bar{V}_t$ is the V_{th} mean, V_{td} is the device V_{th}, the sub-threshold slope parameter (B_1), an extracted parameter (A_1).

Also, it should be noted that the increase in $\sigma(V_t)$ and (V_{th}) accompanying aggressive scaling may prove to be a significant limit for cell performance and SNM.

(iii). Diffusion Leakage

Although diffusion leakage (I_{diff}) did not pose a significant technical challenge for the ULP technology leakage goals, some experimental optimization was required to reach them. Reverse-Bias Diffusion Leakage (RBDL) is a function of defect population within the depletion region and the local stresses arising from sources such as STI(Shallow Trench Isolation) processing parameters and silicide processing [24]. This leakage can be characterized as

$$I_{\text{diff}} = A_2 \exp(E_a/k_T), \qquad \text{Eq. (5)}$$

Where, E_a is roughly equal to $E_g/2$ in the typical junction environment, and A is defined as

$$A_2 = T^{3/2} V^{1/2} \qquad \text{Eq. (6)}$$

The diffusion leakage was minimized by optimizing the source/drain energy, so that the junction depth was deep enough to avoid silicide defects. The relationship between the deep p-well retrograde implant and area diffusion leakage resulted in a reduction of the deep retrograde implant dose for the ULP technology.

(iv). GIDL (Gate Induced Drain Leakage)

The process and device learning required to achieve the ULP technology leakage goals associated with GIDL were significant, because the SRAM array contains a relatively large critical area subject to this mechanism. GIDL and RBDL mechanisms contribute to the cell leakage on both the internal node and bit-line contact regions of the SRAM cell when the bit-lines are held at a high voltage (V_{DD}) during standby mode. Referring again to Fig.1, the gate perimeter associated with the drain of transistors T_2, T_4 (n-FETs) and T_5 (p-FET) contributes GIDL in standby mode. Additionally, as we assume that the bitlines are to be held at a high-voltage (V_{DD}) in standby mode, these mechanisms are also contributing on the bit-line side of both wordline transistors T_1 (n-FET) and T_2 (n-FET).

For the Lightly Doped Drain (LDD) type of structure, GIDL has been shown to be dominated by band-to-band tunneling in the gate-drain overlap region. This leakage mechanism is influenced by many processing parameters such as sidewall oxidation, t_{ox}, spacer width, LDD, silicidation, and halo dopant concentration gradients, depth, and placement. Band-to-Band tunneling, trap-assisted tunneling and interface-state-assisted tunneling may be contributing factors to the overall GIDL observed. Because the gate-bounded leakage is known to be influenced by many processing parameters, more learning with respect to these elements is clearly critical to obtaining ultralow-leakage CMOS.. Band-to-Band tunneling (BBT) has weak temperature dependence and dominates at higher voltages, while band-to-defect tunneling (BDT) has stronger temperature dependence and dominates at lower biasing. High-performance designs tend to have higher fields, which increases the BBT component of GIDL. Defects and interface states are also generated with these higher-dose implants, increasing the BDT component. The ULP device design goal was to reduce GIDL by minimizing the field at the drain edge and at the same time retaining optimum Short-Channel Effect (SCE) control and low series resistance [6].

III. Leakage Current Suppression Techniques

Leakage current suppression techniques can be divided into two groups. One is using the body-bias control [3] and the other is inserting power switches on power lines [1,2]. If only the oxide-tunneling leakage is the main concern, the body-bias control cannot be a solution, because the oxide-tunneling leakage cannot be improved by controlling body-bias voltages. On the contrary, inserting the power switches between the source lines of SRAM cell array and the power lines can control the source-line voltages dynamically resulting in suppressing both sub-threshold and oxide-tunneling leakage. There can be three methods of inserting the power switches on the power lines. The first one is inserting an NMOSFET switch on the V_{SS} power line. Here the V_{SS} and V_{DD} are the power lines of ground and supply voltage, respectively. The second one is inserting a PMOSFET switch on the V_{DD} power line. The third one is inserting both NMOSFET and PMOSFET switches on both the V_{SS} and V_{DD} lines, respectively. All of them are effective in suppressing sub-threshold leakage .In this paper, the three methods mentioned above are compared to find which one is most favorable in terms of suppressing both the oxide-tunneling and sub-threshold leakage in the 65-mn and 45-nm nodes [4]. In addition, the comparison is extended to the future 32-nm node in this paper and the area overheads between the SRAMs with different power gating switches are also discussed in the later section. To reduce oxide-tunneling leakage more, an SRAM circuit with pre-charge voltage lowering is investigated to know how much it can save the leakage for the 65-nm, 45-nm and 32-nm nodes.

(i). SRAM Cell with Power Gating

Fig.2 shows a schematic of the SRAM1 which represents the conventional SRAM cell. Here, the MN1, MN2, MP1, and MP2 form a cross-coupled inverter latch and the MN3 and MN4 are word-line transistors through which the bit lines are connected to the latch. In Fig.2, if the Q and QB nodes have high and low, respectively, the sub-threshold leakage flows through the MP2 and MN1. This leakage through the MP2 and MN1 is called by the cell-leakage. In addition, there is the other leakage current through the MN4 from the BLB node to the VSS. Here, because both the Q and BL nodes have high, sub-threshold leakage does not flow through the MN3. The leakage of the MN4 is called by the bit-line leakage. Both the cell and bit-line leakage currents belong to the sub-threshold component of leakage dissipation. The oxide-tunneling component of leakage can flow through all the transistors as shown in Figure 2. Their leakage paths are indicated by the dotted arrows in Fig. 2.

IACSIT
International Association of Computer Science and Information Technology
WWW.IACSIT.ORG

Fig.3 shows a schematic of the SRAM2, where the MN5 is inserted between the source line of the MN1 and MN2 and the VSS power line. Both the MN6 and MN7 have the diode-connected configuration as shown in Fig 3.

Fig.2 SRAM1 Circuit [9]

When the MN5 is turned off, the source-line voltage of the MN1 and MN2 represented as the V_{SL} is increased from VSS to 2Vt by the MN6 and MN7, thus lowering a retention voltage of the cell by 2Vt. Because the BODY and Drain-Induced Barrier Lowering (DIBL) effects become stronger as the V_{SL} increases higher, the sub-threshold component of leakage can be reduced when the retention voltage is lowered. Next, because voltages across the oxides of the SRAM2 decrease with lowering the retention voltage, their oxide-tunneling leakage currents become smaller with increasing the V_{SL}, too.

Fig.3 SRAM2 Circuit with its Power Switch on the VSS Line [9]

Fig. 4 shows a schematic of the SRAM3, where the MP3 is inserted between the source-line of the MP1 and MP2 and the V_{DD} line. In Fig. 4, when the MP3 is turned off, the source-line voltage of the MP1 and MP2 represented as the V_{SH} drops by $2V_{th}$ through the MN5 and MN6. Thus the retention voltage is reduced from V_{DD} to V_{DD}-2Vt. Like the SRAM2, the BODY and DIBL effects get stronger as the V_{SH} decreases lower. This helps its sub-threshold leakage to be decreased more. Like Fig. 3, because voltages across the oxides of the transistors in Fig. 4 are decreased, their oxide-tunneling leakage currents are reduced, too [9].

The fig. 5 shows a schematic of the SRAM4 which seems like a combination of the SRAM2 and SRAM3. Here, the MN5 and MP3 are inserted between the V_{SL} and V_{SS} and between the V_{DD} and V_{SH}, respectively. The MN6 and MP4 are diode-connected MOSFETs. When the MN5 and MP3 are turned off, its retention voltage defined by voltage difference between the V_{SL} and the V_{SH} is reduced from V_{DD} to V_{DD}-2Vt [9].

Fig.4 SRAM3 Circuit with its Power Switch on the V_{DD} Line [9]

Fig.5 SRAM4 Circuit with its Power Switches on both the VSS and VDD Lines [9]

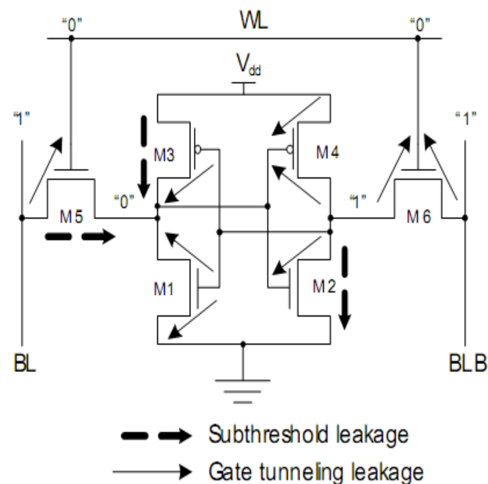
On comparing the 65-nm, 45-nm, and 32-nm Predictive Technology Methods (PTMs) indicates the percentage saving of leakage of the SRAM2 with the 32-nm seems largest among the three 65-nm, 45-nm, and 32-nm nodes. As the technology node becomes smaller, for example, from 65-nm via 45-nm toward 32-nm, the sub-threshold leakage current increases sharply due to its lowered threshold voltage according to the device scaling trend. For the oxide-tunneling leakage, however, the increase in leakage with device scaling looks much smaller than the sub-threshold. This is attributed to the supply voltage lowering compensating the effect of oxide thinning. Hence, the 32-nm node where the sub-threshold component takes the largest portion in the total leakage can save the largest

amount of leakage among the three nodes [9].

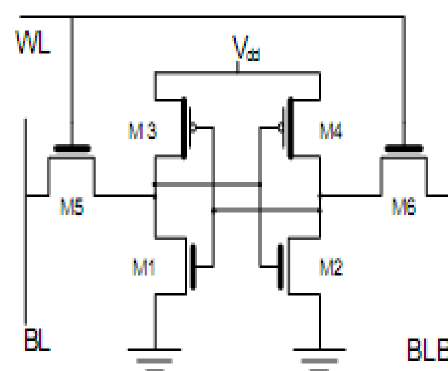
(ii). Dual Vth CMOS 6T-SRAM Cell

To reduce the sub-threshold leakage power consumption of a cell, the threshold voltage of all or some of the transistors of the cell can be increased. When the threshold voltages of all transistors within a cell are increased, the sub-threshold leakage reduction is the highest. However, since this scenario has the worst effect on the read delay of the cell, the number of memory cells that can be changed is low. Thus, we consider other configurations which have smaller sub-threshold leakage reductions, but lower delay penalties. On the other hand, as mentioned in Section III, to reduce the gate tunneling leakage of an SRAM cell, only the oxide thickness of the pull down NMOS transistors and pass-transistors need to be increased. Although this is seemingly desirable from a low power point of view, it is not applicable for all cells in the cell array; thin oxide needs to be used in the cells far from the address decoder and sense amplifiers [6].

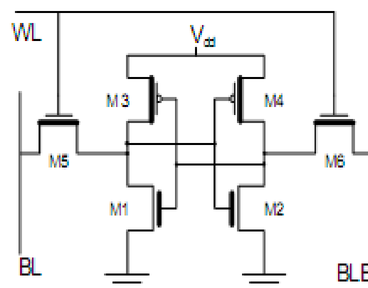
In the following, high V_{th} transistors refer to those transistors whose threshold voltage have been modified by e.g., increasing the channel doping, not the ones whose threshold voltage has been boosted as a result of increasing the oxide thickness. To make the memory cells with more possibilities to manufacture, unlike [8], we use a symmetric cell configuration, which means the symmetrically located transistors within an SRAM cell have the same threshold voltages and oxide thicknesses. Thus, there are 32 different possibilities for assigning high and low threshold voltages and oxide thickness to the transistors within a cell. Since increasing the oxide thickness also increases the threshold voltage of a transistor, we do not increase the oxide thickness and threshold voltage of a transistor at the same time because the delay penalty will be too high. Therefore, the number of different configurations is reduced to eighteen (there are two choices for the pair of PMOS transistors and three choices for each of the pull-down NMOS pair and pass-transistor pair). Each configuration has a different effect on read and write delays of the cells. By simulating all configurations, the dominated ones, i.e., the ones with higher leakage and longer read/write delay than at least one other configuration are eliminated. Five configurations remain as shown in Fig. 6. [14]. The decrease in leakage power consumption of each configuration, compared to the initial configuration where all threshold voltages are low and all oxide thicknesses are thin, is shown in Fig. 6. One can see that the C1 cell, for which all four NMOS transistors have thick-Tox and the PMOS transistors have a high threshold voltage, exhibits 90% lower leakage compared to the initial cell C0, for which all transistors have low-T_{ox} and low-V_{th}.



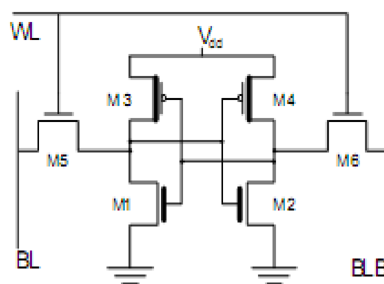
C0: SRAM Cell with Low Tox and Low Vth



C1: M3&M4 High Vth, M1, M2, M5, M6 are High Tox Transistors

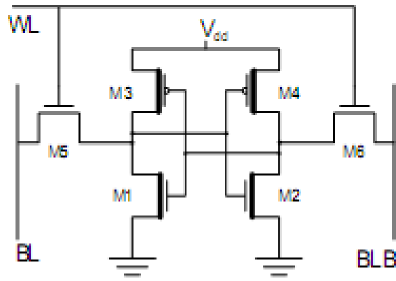


C2: M3, M4, M5, M6 High Vth, M1, M2, are High Tox Transistors

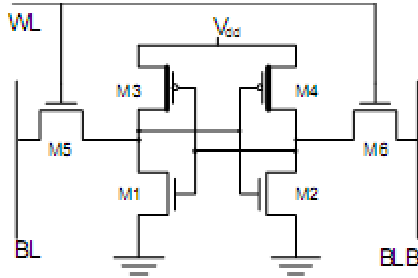


C3: M3, M4, High Vth, M1, M2, are High Tox Transistors

IACSIT
International Association of
Computer Science and Information Technology
WWW.IACSIT.ORG



C4: M1, M2, M3, M4, M5, M6 High Vth Transistors



C5: M3, M4 High Vth Transistors

Fig.6. Various Combinations of SRAM Cells with High Vth and High Tox [14]

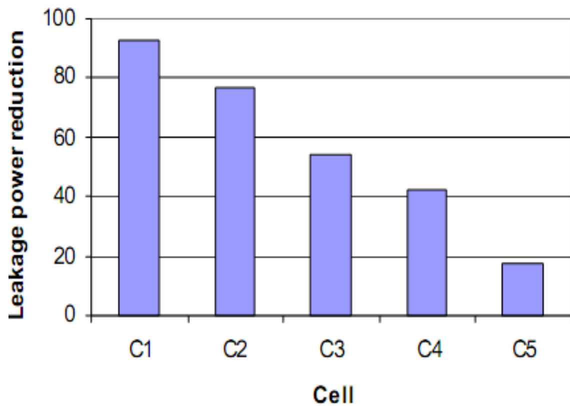


Fig.7. Leakage Power Reduction of Various Cells [14]

The configurations shown in Fig.7, have different leakage power consumptions. The decrease in leakage power consumption of each configuration, compared to the initial configuration where all threshold voltages are low and all oxide-thicknesses are thin, is shown in Fig.6. It can seen that the C1 cell, for which all four NMOS transistors have thick-Tox and the PMOS transistors have a high threshold voltage, exhibits 90% lower leakage compared to the initial cell C0, for which all transistors have low-T_{ox} and low-V_{th} [14].

(iii). Stacking Technique for 6T SRAM Cell

It has been observed that the stacking of two off transistors can significantly reduce leakage power than a single off transistor [3]. Increasing the source voltage of NMOS transistor reduces sub-threshold leakage current given by equation 1, exponentially due to negative V_{gs}, lowered signal rail, reduced DIBL and body effect. As the drain-to-source potential decreases, it results in less drain-induced barrier lowering (DIBL). As a result the sub-threshold leakage is further reduced. This phenomenon is the "stacking effect." This technique is useful in reducing the leakage current. The fig.8 shows the power dissipation in a 6 T SRAM cell v/s the number of stacks [20].

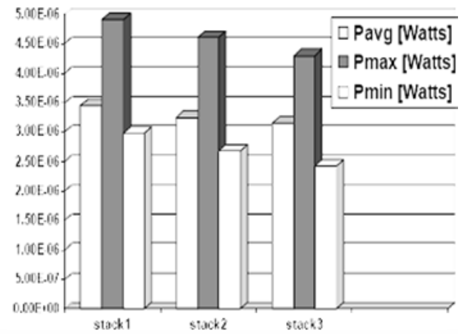


Fig.8 Stacking Analysis with power consumption [20]

IV. A COMPARISON IN DIFFERENT SRAM CELLS (SRAM1, SRAM2, SRAM3, SRAM4)

TABLE1.ANALYSIS OF LEAKAGE CURRENTS IN VARIOUS SRAM CELLS

Type of SRAM	Technology (nm)	Temperature (^{0}C)	Total Leakage (nA)	Comment/ Outcomes
SRAM1	65	25	18.15	A portion of the oxide-tunneling component in leakage increasing with the temperature go down. On the contrary, the sub-threshold leakage becomes more dominant at higher temperatures. Hence at lower temperature the total leakage is less.At higher temperatures such as 25°C and 100°C, however, the total leakage of the SRAM2 becomes smaller than the SRAM4. This is caused from the SRAM2 has the BODY effect on the MN1 and MN2 stronger than the SRAM4. Because the MN1 and MN2 are wider than the other transistors, suppressing leakage of the MN1 and MN2 gives the largest impact on lowering the total leakage dissipation of the
	65	100	53.07	
SRAM2	65	25	2.14	
	65	100	5.96	
SRAM3	65	25	6.42	
	65	100	21.87	
SRAM4	65	25	2.4	
	65	100	7.37	

				SRAM2.
SRAM1	45	25	26.9	At 100°C with the 45-nm PTM, the SRAM2, SRAM3, and SRAM4 can save their leakage currents as large as 92%, 64.6%, and 90.1% of the leakage of the SRAM1, respectively. Among the SRAM2, SRAM3, and SRAM4, the SRAM2 saves the largest amount of leakage than the other two because its subthreshold leakage is decreased most. Concerning the oxide-tunneling leakage, however, the SRAM4 has smaller values than the SRAM2, though the total leakage of the SRAM2 is smaller than the SRAM4. For the temperature of 25°C the results are almost similar with the 100°C, here is the leakage saving of the SRAM2 is larger than that of the SRAM4 only by 1.2% at 25°C whereas the difference is 1.9% at 100°C. As the temperature becomes lower, the sub-threshold leakage currents of both the SRAM2 and SRAM4 decrease thus difference in savings between them becoming smaller, too.
	45	100	79.6	
SRAM2	45	25	2.08	
	45	100	6.35	
SRAM3	45	25	8.49	
	45	100	28.15	
SRAM4	45	25	2.41	
	45	100	7.85	
SRAM1	32	25	52.48	Among the SRAM2, SRAM3, and SRAM4, the SRAM2 saves the largest amount of leakage than the other two because its subthreshold leakage is decreased most.
	32	100	143.6	
SRAM2	32	25	2.385	
	32	100	7.699	
SRAM3	32	25	13.99	
	32	100	41.71	
SRAM4	32	25	2.73	
	32	100	8.99	

V. Conclusion

As the technology is scaled day-by-day, the leakage is becoming a prime concern in the area of integrated circuit design. Low power memory is in great demand today for various applications and so we try to review the SRAM with low leakage current. As the technology is scaling day by day so the leakage reduction method is according to the new predictive technology. In this work, we compare the various SRAM circuits to get low leakage current at the new and different levels of device scaling. They are the conventional SRAM1, SRAM2 with power gating on the V_{SS} line, the SRAM3 with power gating on the V_{DD} line, and the SRAM4 with both on the V_{DD} and V_{SS} lines, respectively. Among the four SRAM, the SRAM2 shows the smallest amount of leakage, ie., 2.73nA, because its sub-threshold leakage is most suppressed by its BODY and DIBL effects. Also, the study of the change in the threshold voltage or the thickness of gate-oxide of some transistor cells is done to decrease the leakage current without degrading its performance. By using five different configurations SRAM1,SRAM2,SRAM3,SRAM4 for the SRAM cells, we have achieved a low-leakage SRAM without scarifying performance and area is achieved.

Acknowledgment

The authors are very grateful to their respective organizations for encouragement and support.

Refrences

[1] A. Agarwal, H. Li, and K. Roy, “A single Vt low-leakage gated-ground cache for deep submicron,” IEEE Journal of Solid-State Circuits, vol. 38, no. 2, pp. 319-328, 2003.

[2] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45nmdesign exploration," International Symposium on Quality Electronic Design, pp. 585-590, 2006.

[3] H. Kawaguchi, Y. Iataka, and T. Sakurai, “Dynamic leakage cut-off scheme for low-voltage SRAM’s,” Technical digest of Symposium on VLSI circuits, pp. 140-141, June 1998.

[4] D. Lee, D. Kwak, and K. Min, “Comparative Study on SRAMs for Suppressing Both Oxide-Tunneling Leakage and Subthreshold Leakage in Sub-70-nm Leakage Dominant VLSIs,” 20th International VLSI Design Conference, pp. 632-637, Jan. 2007.

[5] R. W. Mann etal., “Ultra Low Power SRAM technology”, IBM J. RES. & DEV. VOL. 47 NO. 5/6 September/November 2003.

[6] V. De et al., “Techniques for leakage power reduction in Design of High-Performance Microprocessor Circuit”, A. Chandrakasan, W. J. Bowhill, and F. Fox, Eds. Piscataway, NJ: IEEE, 2001, pp. 285-308.

[7] K. Zhang et al., “SRAM design on 65-nm CMOS technology with dynamic sleep transistor for leakage reduction,” IEEE J. Solid-State Circuits, vol. 40, no. 4, Apr. 2005, pp. 895-901.

[8] Shilpi Birla, Neeraj Kr. Shukla, R.K. Singh, and Manisha Pattanaik., “Analysis of the Data Stability and Leakge Power in the Various SRAM Cell Topologies”, International Journal of Engineering Science and Technology Vol. 2(7), 2010, 2936-2944.

[9] Duk-Hyung Lee, “Comparative Study on Leakage Current of Power-Gated SRAMs for 65-nm, 45-nm, and 32-nm Technology Nodes”, Journal of Computers, Vol. 3, No. 3, pp.39-47, MARCH 2008.

[10] Jinhui Chen Clark, L.T. Tai-Hua Chen, “An Ultra-Low-Power Memory with a Subthreshold Power Supply Voltage”, Solid-State Circuits, IEEE Journal, vol.41, Oct 2006, Issue: 10, pp- 2344-2353.

[11] Hamzaoglu, F.; Zhang, K.; Yih Wang; Ahn, H.J.; Bhattacharya, U.; Zhanping Chen; Yong-Gee Ng; Pavlov, A.; Smits, K.; Bohr, M , “A 3.8 GhZ3 Mb SRAM Design With Dynamic Stability Enhancement and Leakage Reduction in 45 nm High-k Metal Gate CMOS Technology” ,Solid-State Circuits, IEEE Journal ,vol. 44 , no. 1, 2009, pp.148 – 154.

[12] Kushidak., SuzukiA., etal, “A 0.7 V Single-Supply SRAM With 0.495 μm^2 in 65 nm Technology Utilizing Self-Write-Back Sense Amplifier and Cascaded Bit Line Scheme, , Solid-State Circuits, IEEE Journal, vol. 44, No. 4, April. 2009, pp.1192-1198.

IACSIT
International Association of Computer Science and Information Technology
WWW.IACSIT.ORG

[13] Yeonbae Chung, Seung-Ho Song, "Implementation of low-voltage static RAM with enhanced data stability and circuit speed", Microelectronics Journal, Vol. 40, Issue 6, June 2009, pp. 944-951.
[14] Behnam Amelifard, et al. "Reducing the Sub-threshold and gate tunneling leakage of SRAM cells using dual Vt and Dual Tox assignment", Fujitsu Labs of America, 2008.
[15] A. Ono, R. Ueno, and I. Sakai, "TED Control Technology for Suppression of Reverse Narrow Channel Effect in 0.1µm MOS Devices," IEDM Tech. Digest, 1997, pp. 227–230.
[16] J. Kim, T. Kim, J. Park, W. Kim, B. Hong, and G. Yoon, "A Shallow Trench Isolation Using Nitric Oxide (NO)-Annealed Wall Oxide to Suppress Inverse Narrow Width Effect," IEEE Electron Device Lett. 21, No. 12, 575–577 (2000).
[17] A. Asenov and S. Saini, "Suppression of Random Dopant Induced Threshold Voltage Fluctuations in Sub-0.1µm MOSFET's with Epitaxial and Delta-Doped Channels," IEEE Trans. Electron Devices 46, No. 8, 1718 –1724 (1999).
[18] A. J. Bhavnagarwala, X. Tang, and J. Meindl, "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability," IEEE J. Solid-State Circuits 36, No. 4, 658–665 (2001).
[19] K. Takeuchi, "Channel Size Dependence of Dopant-Induced Threshold Voltage Fluctuation," Digest of Technical Papers, Symposium on VLSI Technology, 1998, p. 72.
[20] S.S.Rathod, S.Dasgupt, and Ashok Saxena , "Investigation of Stack as a Low Power Design Technique for 6-T SRAM Cell. Proc.IEEE TENCON, Nov.18-21,Universityof Hyderabad, 2008, pp 1-5.

[1]**Neeraj Kr. Shukla** (IEEE, IACSIT,IAENG, IETE, IE, CSI, ISTE), a Ph.D. Scholar at the UK Technical University, Dehradun (Uttarakhand) India is an Asst. Professor in the Department of Electrical, Electronics & Communication Engineering, ITM University, Gurgaon, (Haryana) India. He has received his M.Tech. (Electronics Engineering) and B.Tech. (Electronics & Telecommunication Engineering) Degrees from the J.K. Institute of Applied Physics & Technology, University of Allahabad, Allahabad (Uttar Pradesh) India in the year of 1998 and 2000, respectively. His main research interests are in Low-Power Digital VLSI Design and its Multimedia Applications, Open Source EDA, and RTL Design.

[2]**Shilpi Birla** (IACSIT, IAENG), a Ph.D. Scholar at the UK Technical University, Dehradun (Uttarakhand) India is an Asst. Professor in the Department of Electronics & Communication Engineering, Sir Padampat Singhania University, Udaipur (Rajasthan) India. She has received her M.Tech. (VLSI Design) and B.E. (Electronics & Communication Engineering) Degrees from the University of Rajasthan, Jaipur (Rajasthan) India and MITS University, Laxmangarh, (Rajasthan) India, respectively. Her main research interests are in Low-Power VLSI Design and its Multimedia Applications, RF-SiP, and Low-Power CMOS Circuit Design.

[3]**R.K. Singh** (IAENG, ACEEE, IE, ISTE), Professor in the Department of Electronics & Communication Engineering, VCT-Kumaon Engineering College, Dwarahat, Almora (UK) India. He is being honored with the Ph.D. in Electronics Engineering in the Year 2003 from the University of Allahabad, Allahabad (Uttar Pradesh), India. He has received his M.E. (Electronics & Control Engineering) in 1992 from BITS, Pilani and B.E. (Electronics & Communication Engineering) in 1990 from Marathawada University, India. He has authored several text-books in the field of VLSI Design, Basic Electronics, and Opto-Electronics. He has worked at various capacities as, the Principle, Kumaon Engineering College, Dwarahat in the year 2003-04, Director (O), Directorate of Technical Education, Uttaranchal in the year 2005, and Joint Director, State Project Facilitation Unit, Dehradun for the World Bank TEQIP Project. He is also the recipient of couple of prestigious awards, e.g., Rastriya Samman Puruskar, Jewel of India Award, Rastriya Ekta Award, Life Time Achievement Award, and Arch of Excellence Award. His current areas of interest are VLSI Design, Opto-Electronics and its applications.

[4]**Manisha Pattanaik** (WSEAS, IE, ISTE) has been honored the Ph.D. from Indian Institute of Technology (IIT) Kharagpur, India in the field of VLSI Design from the Department of Electronics and Electrical Communication Engineering in the year 2004. Currently she is an Assistant Professor (VLSI Group) at ABV-India Institute of Information Technology & Management (ABV-IIITM), Gwalior, (Madhya Pradesh), India. She has been awarded various scholarships, e.g., National Scholarships, Merit Scholarships and MHRD Fellowships. She shared the responsibility in the capacity of referee for IEEE International Conferences on VLSI Design for two consecutive years, 2003-04. Her areas of interest are Leakage Power Reduction of Nano-Scale CMOS Circuits, Characterization of Logic Circuit Techniques for Low-Power/Low-Voltage and High performance analog & digital VLSI applications and CAD of VLSI Design.