Abstract—For mobile and multimedia applications of SRAMs, there is a strong need to reduce standby current leakages while keeping the memory cell data unchanged. To meet this objective, various techniques have been developed to reduce the leakage current at the process/device, circuit, architecture, and algorithmic levels. The traditional 6T CMOS SRAMs face many challenges in deep-submicron (DSM) technologies for low supply voltage (VDD) operation. Predictions suggest that process variations will limit standard 90nm SRAMs to around 0.7V operation because of the Static Noise Margin (SNM) degradation and write margin, also a VDD of 0.7V is reported for a 65nm SRAM. This work discusses some of the schemes that minimize the cell leakage regardless of the process fluctuations and the environmental conditions. Various SRAM leakage currents identify the suitable schemes for 6T SRAM sub-threshold operation at device and circuit levels for optimal sub-threshold circuit designs and provides an effective roadmap for digital circuit designers who are interested to work with ultra-low-power applications in CMOS technology.

Index Terms—DSM (Deep Sub-Micron), Power Gating, SNM (Static Noise Margin), Sub-threshold Operation, Data Retention.

I. INTRODUCTION

Rising demand for multimedia rich applications like portable and handheld devices have tremendously increases the need for large and high performance memories like the Static Random Access Memory (SRAM). The on-die cache memory occupies a large portion of the silicon area, i.e., of the total chip area. It also plays a significant role in overall power consumption of the multimedia application. Due to continuously scaling of the CMOS devices, it is possible to have a high packaging density which helps in reducing the overall Si area. To minimize the overall power consumption, the first design factor loved by the designer community is the supply voltage (VDD) reduction. This reduction in VDD, though appreciates the power consumption, results in two important concerns, the data stability and the leakage power. The leakage current composes nearly 40% of total power consumption in today’s high performance chip. There are several leakage reduction techniques has been introduced by the researcher community but each has to be checked and verified according to the circuit techniques and target technology without loosing the concerns in data stability, delay, etc.

This paper provides an analytical and comparative roadmap to explains which are the main components of leakage currents, and how they can be minimized using various device and circuit techniques. These techniques incorporate various biasing schemes and other methodologies that depend on the number of transistor in the CMOS SRAM Cells.

II. SRAM CELL LEAKAGE MECHANISM

Fig.1 shows schematically the significant parametric cell leakage paths and mechanisms operating in the 6T SRAM. For each leakage mechanism and resolving the leakage to the given cell dimensions, the total cell and/or array leakage can be calculated effectively and the expected array leakage can be estimated adequately. In Fig.1, for the arbitrary state selected, the internal node on the left side of the latch is maintained at ground while the node on the right is held at VDD by the operation of the cross-coupled latch. The intent of this section is to describe in brief the critical parametric leakage sources within the cell, derived from this latched configuration that corresponds to memory array standby mode. Although the schematic in Fig. 3 shows the gate-leakage to substrate for transistor T3 and to the n-well for T6, it needs be pointed out that the majority of the carriers are swept to the source nodes by the applied field.

In this paper, we review the critical parametric leakage mechanisms operating within the SRAM cell and describe how the mechanism was addressed in the described Ultra Low Power (ULP) technology. Five dominant parametric mechanisms to be addressed are threshold voltage optimization, gate tunneling leakage, sub-threshold leakage, reverse-bias diffusion leakage, and gate-induced drain (GIDL) leakage. Of all these mechanisms, mostly development efforts were addressed threshold voltage optimization and GIDL reduction. Some of the major leakage currents that play an important role in the power consumption of the chip are being discussed here.
The gate tunneling leakage mechanism is active for the n-FET (T3) and p-FET (T6) sites shown in Fig. 1. For the purpose described in this paper, the leakage is generally found to be adequately modeled for a given voltage as a function of gate-oxide thickness from the empirical relationship [5], for both the n-FETs and p-FETs.

\[ I_{g}(t_{ox}) = A_0 \exp(-Bt_{ox}) \]  

Eq. (1)

Because this mechanism is governed by quantum-mechanical tunneling, this mechanism is virtually temperature-independent while other leakage mechanisms dominate at higher temperatures. This mechanism was found to establish the minimum gate-oxide thickness for the technology on the basis of the established lower-temperature leakage targets.

(ii). \( V_t \) and Sub-threshold Leakage Current

For the narrow-width devices used in the SRAM cell, the off-current of the device is elevated compared with that of a wide device because of the narrow-channel effect (NCE). The effective reduction in \( V_{th} \) associated with geometric constraints of the narrow channel is a significant challenge for future Ultra Low-Power (ULP) technologies. In the example shown, the \( I_{source} \) at zero gate bias is below 10 fA/µm at room temperature and below 600 fA/µm at 85°C for both n-FET and p-FET devices. At 25°C, it is clear that the drain current at room temperature is dominated by Gate Induced Drain Leakage (GIDL). Unlike gate-oxide tunneling leakage, sub-threshold device off-current leakage is strongly temperature-dependent and is typically the dominant leakage mechanism at higher temperatures.

Fig.1 shows the three transistors in which this mechanism is actively contributing to the standby leakage when the SRAM array is in the standby state. In the example given in Fig. 2, the internal node transistors T4 (n-FET) and T5 (p-FET) and the wordline transistor T1 (n-FET) are being held in the off state and have a drain-to-source voltage of \( V_{DD} \). Since it is the most common for the bitlines to be held high (at \( V_{DD} \)) in standby mode, this is the mode shown for the sake of discussion. However, it is worth pointing out that if the bitlines were held low (at ground), there would still be three devices in the cell contributing to the off-state leakage, since the internal nodes of the SRAM cell are held in opposite states. The off-state leakage can be adequately characterized given the subthreshold slope parameter \((B_1)\), an extracted parameter \((A_1)\) and threshold voltage \((V_t)\) for both the n-FET and the p-FET with the following relationship [5],

\[ I_{off}(V_t, T) = C(T)A_1e^{(B_1V_t)} \]  

Eq. (2)

Where, \( C(T) \) is expressed as,

\[ C(T) = 10^{(V_tS)\left(-\frac{1}{509}(T-298)\frac{1}{T}298\right)} \]  

Eq. (3)

Where, \( S \) is the sub-threshold slope, \( Y \) is the slope of the \( V_{th} \) as a function of temperature, and \( T \) is the temperature in degrees Kelvin.

Because of the obvious importance of \( V_t \)control for both array leakage and cell stability, two additional topics which relate to \( V_{th} \)control must be addressed for ULP technologies. These include the effect of device width on \( V_t \), referred to as Narrow-Channel Effect (NCE) [15,16] and the treatment of statistical variations in \( V_{th} \) in narrow devices. Both of these factors become increasingly important for the 0.13µm node and below. While this explanation is generally accepted for the n-FET. So far, no complete explanation has been proposed for the observed NCE in the ULP p-FET device. The observed p-FET behavior appears to be unique to the ULP technologies. As for the high-performance devices the p-FET NCE typically results in a slightly higher \( V_t \) with narrower channels. As a result of this phenomenon, the threshold voltages must be set higher than one might assume on the basis of the measured wide device off-current in order to achieve the cell leakage targets. It is well known that the statistical variation in \( V_{th} \) will become an increasing concern as devices continue to scale [18,19]. This is due to not only to the physical dimension tolerances but also to statistical variations in channel dopant associated with the reduction in channel area. This variation can be compounded in the SRAM cell by \( V_{th} \) variations associated with overlay tolerances and corner-rounding effects due to aggressive scaling to achieve maximum density for the cell. Because of the exponential relationship of \( I_{off} \) with \( V_{th} \), the contribution of the devices in the array with lower threshold voltage must be accounted for in calculating the overall array leakage [5,7].

The array leakage increase associated with the variation in the standard deviation of \( V_{th} \), i.e., \((V_{th})\), can be estimated by means of the following equation [5],

\[ I_{std}[V_{th}] = \int_{V_{th}}^{V_{th}+\sigma(V_{th})} \frac{1}{\sqrt{2\pi}\sigma(V_{th})} e^{-\frac{(1/2)\sigma(V_{th})^2[V_{th}]}{\sigma(V_{th})^2}} A_1e^{(-B_1V_t)} dV_{th} \]

\[ = \frac{A_1e^{(-B_1V_t)}}{\sqrt{2\pi}\sigma(V_{th})^2} \]  

Eq. (4)

Where, \( V_{th} \) is the \( V_{th} \) mean, \( V_{std} \) is the device \( V_{th} \), the subthreshold slope parameter \((B_1)\), an extracted parameter \((A_1)\).
Also, it should be noted that the increase in $\sigma(V_{t1})$ and $(V_{th})$, accompanying aggressive scaling may prove to be a significant limit for cell performance and SNM.

(iii). Diffusion Leakage

Although diffusion leakage ($I_{diff}$) did not pose a significant technical challenge for the ULP technology leakage goals, some experimental optimization was required to reach them. Reverse-Bias Diffusion Leakage (RBDL) is a function of defect population within the depletion region and the local stresses arising from sources such as STI(Shallow Trench Isolation) processing parameters and silicide processing [24]. This leakage can be characterized as

$$I_{diff} = A_2 \exp\left(\frac{E_g}{kT}\right),$$

Eq. (5)

Where, $E_g$ is roughly equal to $E_g/2$ in the typical junction environment, and $A$ is defined as

$$A_2 = T^{3/2}V^{1/2}$$

Eq. (6)

The diffusion leakage was minimized by optimizing the source/drain energy, so that the junction depth was deep enough to avoid silicide defects. The relationship between the deep p-well retrograde implant and area diffusion leakage resulted in a reduction of the deep retrograde implant dose for the ULP technology.

(iv). GIDL (Gate Induced Drain Leakage)

The process and device learning required to achieve the ULP technology leakage goals associated with GIDL were significant, because the SRAM array contains a relatively large critical area subject to this mechanism. GIDL and RBDL mechanisms contribute to the cell leakage on both the internal node and bit-line contact regions of the SRAM cell when the bit-lines are held at a high voltage $(V_{DD})$ during standby mode. Referring again to Fig.1, the gate perimeter associated with the drain of transistors $T_2$, $T_3$ (n-FETs) and $T_5$ (p-FET) contributes GIDL in standby mode. Additionally, as we assume that the bitlines are to be held at a high-voltage $(V_{DD})$ in standby mode, these mechanisms are also contributing on the bit-line side of both wordline transistors $T_1$ (n-FET) and $T_3$ (n-FET).

For the Lightly Doped Drain (LDD) type of structure, GIDL has been shown to be dominated by band-to-band tunneling in the gate-drain overlap region. This leakage mechanism is influenced by many processing parameters such as sidewall oxidation, $t_{ox}$, spacer width, LDD, silicidation, and halo dopant concentration gradients, depth, and placement. Band-to-Band tunneling, trap-assisted tunneling and interface-state-assisted tunneling may be contributing factors to the overall GIDL observed. Because the gate-bounded leakage is known to be influenced by many processing parameters, more learning with respect to these elements is clearly critical to obtaining ultralow-leakage CMOS. Band-to-Band tunneling (BBT) has weak temperature dependence and dominates at higher voltages, while band-to-defect tunneling (BDT) has stronger temperature dependence and dominates at lower biasing. High-performance designs tend to have higher fields, which increases the BBT component of GIDL. Defects and interface states are also generated with these higher-dose implants, increasing the BDT component. The ULP device design goal was to reduce GIDL by minimizing the field at the drain edge and at the same time retaining optimum Short-Channel Effect (SCE) control and low series resistance [6].

III. LEAKAGE CURRENT SUPPRESSION TECHNIQUES

Leakage current suppression techniques can be divided into two groups. One is using the body-bias control [3] and the other is inserting power switches on power lines [1, 2]. If only the oxide-tunneling leakage is the main concern, the body-bias control cannot be a solution, because the oxide-tunneling leakage cannot be improved by controlling body-bias voltages. On the contrary, inserting the power switches between the source lines of SRAM cell array and the power lines can control the source-line voltages dynamically resulting in suppressing both sub-threshold and oxide-tunneling leakage. There can be three methods of inserting the power switches on the power lines. The first one is inserting an NMOSFET switch on the V_{SS} power line. Here the V_{SS} and V_{DD} are the power lines of ground and supply voltage, respectively. The second one is inserting a PMOSFET switch on the V_{DD} power line. The third one is inserting both NMOSFET and PMOSFET switches on both the V_{SS} and V_{DD} lines, respectively. All of them are effective in suppressing sub-threshold leakage. In this paper, the three methods mentioned above are compared to find which one is most favorable in terms of suppressing both the oxide-tunneling and sub-threshold leakage in the 65-nm and 45-nm nodes [4]. In addition, the comparison is extended to the future 32-nm node in this paper and the area overheads between the SRAMs with different power gating switches are also discussed in the later section. To reduce oxide-tunneling leakage more, an SRAM circuit with pre-charge voltage lowering is investigated to know how much it can save the leakage for the 65-nm, 45-nm and 32-nm nodes.

(i). SRAM Cell with Power Gating

Fig.2 shows a schematic of the SRAM1 which represents the conventional SRAM cell. Here, the MN1, MN2, MP1, and MP2 form a cross-coupled inverter latch and the MN3 and MN4 are word-line transistors through which the bit lines are connected to the latch. In Fig.2, if the Q and QB nodes have high and low, respectively, the sub-threshold leakage flows through the MP2 and MN1. This leakage through the MP2 and MN1 is called by the cell-leakage. In addition, there is the other leakage current through the MN4 from the BLB node to the VSS. Here, because both the Q and BL nodes have high, sub-threshold leakage does not flow through the MN3. The leakage of the MN4 is called by the bit-line leakage. Both the cell and bit-line leakage currents belong to the sub-threshold component of leakage dissipation. The oxide-tunneling component of leakage can flow through all the transistors as shown in Figure 2. Their leakage paths are indicated by the dotted arrows in Fig. 2.
Fig. 3 shows a schematic of the SRAM2, where the MN5 is inserted between the source line of the MN1 and MN2 and the VSS power line. Both the MN6 and MN7 have the diode-connected configuration as shown in Fig 3.

When the MN5 is turned off, the source-line voltage of the MN1 and MN2 represented as the $V_{SL}$ is increased from VSS to 2Vt by the MN6 and MN7, thus lowering a retention voltage of the cell by 2Vt. Because the BODY and Drain-Induced Barrier Lowering (DIBL) effects become stronger as the $V_{SL}$ increases higher, the sub-threshold component of leakage can be reduced when the retention voltage is lowered. Next, because voltages across the oxides of the SRAM2 decrease with lowering the retention voltage, their oxide-tunneling leakage currents become smaller with increasing the $V_{SL}$, too.

Fig. 4 shows a schematic of the SRAM3, where the MP3 is inserted between the source-line of the MP1 and MP2 and the $V_{DD}$ line. In Fig. 4, when the MP3 is turned off, the source-line voltage of the MP1 and MP2 represented as the $V_{SH}$ drops by 2Vth through the MN5 and MN7. Thus the retention voltage is reduced from $V_{DD}$ to $V_{DD}-2Vt$. Like the SRAM2, the BODY and DIBL effects get stronger as the $V_{SH}$ decreases lower. This helps its sub-threshold leakage to be decreased more. Like Fig. 3, because voltages across the oxides of the transistors in Fig. 4 are decreased, their oxide-tunneling leakage currents are reduced, too [9].

The fig. 5 shows a schematic of the SRAM4 which seems like a combination of the SRAM2 and SRAM3. Here, the MN5 and MP3 are inserted between the $V_{SL}$ and $V_{SS}$ and between the $V_{DD}$ and $V_{SH}$, respectively. The MN6 and MP4 are diode-connected MOSFETs. When the MN5 and MP3 are turned off, its retention voltage defined by voltage difference between the $V_{SL}$ and the $V_{SH}$ is reduced from $V_{DD}$ to $V_{DD}-2Vt$ [9].

On comparing the 65-nm, 45-nm, and 32-nm Predictive Technology Methods (PTMs) indicates the percentage saving of leakage of the SRAM2 with the 32-nm seems largest among the three 65-nm, 45-nm, and 32-nm nodes. As the technology node becomes smaller, for example, from 65-nm via 45-nm toward 32-nm, the sub-threshold leakage current increases sharply due to its lowered threshold voltage according to the device scaling trend. For the oxide-tunneling leakage, however, the increase in leakage with device scaling looks much smaller than the sub-threshold. This is attributed to the supply voltage lowering compensating the effect of oxide thinning. Hence, the 32-nm node where the sub-threshold component takes the largest portion in the total leakage can save the largest
amount of leakage among the three nodes [9].

(ii). Dual Vth CMOS 6T-SRAM Cell

To reduce the sub-threshold leakage power consumption of a cell, the threshold voltage of all or some of the transistors of the cell can be increased. When the threshold voltages of all transistors within a cell are increased, the sub-threshold leakage reduction is the highest. However, since this scenario has the worst effect on the read delay of the cell, the number of memory cells that can be changed is low. Thus, we consider other configurations which have smaller sub-threshold leakage reductions, but lower delay penalties. On the other hand, as mentioned in Section III, to reduce the gate tunneling leakage of an SRAM cell, only the oxide thickness of the pull down NMOS transistors and pass-transistors need to be increased. Although this is seemingly desirable from a low power point of view, it is not applicable for all cells in the cell array; thin oxide needs to be used in the cells far from the address decoder and sense amplifiers [6].

In the following, high $V_{th}$ transistors refer to those transistors whose threshold voltage have been modified by e.g., increasing the channel doping, not the ones whose threshold voltage has been boosted as a result of increasing the oxide thickness. To make the memory cells with more possibilities to manufacture, unlike [8], we use a symmetric cell configuration, which means the symmetrically located transistors within an SRAM cell have the same threshold voltages and oxide thicknesses. Thus, there are 32 different possibilities for assigning high and low threshold voltages and oxide thickness to the transistors within a cell. Since increasing the oxide thickness also increases the threshold voltage of a transistor, we do not increase the oxide thickness and threshold voltage of a transistor at the same time because the delay penalty will be too high. Therefore, the number of different configurations is reduced to eighteen (there are two choices for the pair of PMOS transistors and three choices for each of the pull-down NMOS pair and pass-transistor pair). Each configuration has a different effect on read and write delays of the cells. By simulating all configurations, the dominated ones, i.e., the ones with higher leakage and longer read/write delay than at least one other configuration are eliminated. Five configurations remain as shown in Fig. 6. [14]. The decrease in leakage power consumption of each configuration, compared to the initial configuration where all threshold voltages are low and all oxide thicknesses are thin, is shown in Fig. 6. One can see that the C1 cell, for which all four NMOS transistors have thick-Tox and the PMOS transistors have a high threshold voltage, exhibits 90% lower leakage compared to the initial cell C0, for which all transistors have low-$T_{ox}$ and low-$V_{th}$. 

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**C0: SRAM Cell with Low Tox and Low Vth**

**C1: M3&M4 High Vth, M1, M2, M5, M6 are High Tox Transistors**

**C2: M3, M4, M5, M6 High Vth, M1, M2, are High Tox Transistors**

**C3: M3, M4, High Vth, M1, M2, are High Tox Transistors**
C4: M1, M2, M4, M5, M6 High Vth Transistors

C5: M3, M4 High Vth Transistors

Fig.6. Various Combinations of SRAM Cells with High Vth and High Tox [14]

The configurations shown in Fig.7, have different leakage power consumptions. The decrease in leakage power consumption of each configuration, compared to the initial configuration where all threshold voltages are low and all oxide-thicknesses are thin, is shown in Fig.6. It can be seen that the C1 cell, for which all four NMOS transistors have thick-Tox and the PMOS transistors have a high threshold voltage, exhibits 90% lower leakage compared to the initial cell C0, for which all transistors have low-Tox and low-Vth [14].

(iii) Stacking Technique for 6T SRAM Cell

It has been observed that the stacking of two off transistors can significantly reduce leakage power than a single off transistor [3]. Increasing the source voltage of NMOS transistor reduces sub-threshold leakage current given by equation 1, exponentially due to negative Vgs, lowered signal rail, reduced DIBL and body effect. As the drain-to-source potential decreases, it results in less drain-induced barrier lowering (DIBL). As a result the sub-threshold leakage is further reduced. This phenomenon is the “stacking effect.” This technique is useful in reducing the leakage current. The fig.8 shows the power dissipation in a 6 T SRAM cell v/s the number of stacks [20].

IV. A COMPARISON IN DIFFERENT SRAM CELLS (SRAM1, SRAM2, SRAM3, SRAM4)

<table>
<thead>
<tr>
<th>Type of SRAM</th>
<th>Technology (nm)</th>
<th>Temperature (°C)</th>
<th>Total Leakage (mA)</th>
<th>Comment/Outcomes</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM1</td>
<td>65</td>
<td>25</td>
<td>18.15</td>
<td>A portion of the oxide-tunneling component in leakage increasing with the temperature go down. On the contrary, the sub-threshold leakage becomes more dominant at higher temperatures. Hence at lower temperature the total leakage is less. At higher temperatures such as 25°C and 100°C, however, the total leakage of the SRAM2 becomes smaller than the SRAM4. This is caused from the SRAM2 has the BODY effect on the MN1 and MN2 stronger than the SRAM4. Because the MN1 and MN2 are wider than the other transistors, suppressing leakage of the MN1 and MN2 gives the largest impact on lowering the total leakage dissipation of the</td>
</tr>
<tr>
<td></td>
<td>65</td>
<td>100</td>
<td>53.07</td>
<td></td>
</tr>
<tr>
<td>SRAM2</td>
<td>65</td>
<td>25</td>
<td>2.14</td>
<td></td>
</tr>
<tr>
<td></td>
<td>65</td>
<td>100</td>
<td>5.96</td>
<td></td>
</tr>
<tr>
<td>SRAM3</td>
<td>65</td>
<td>25</td>
<td>6.42</td>
<td></td>
</tr>
<tr>
<td></td>
<td>65</td>
<td>100</td>
<td>21.87</td>
<td></td>
</tr>
<tr>
<td>SRAM4</td>
<td>65</td>
<td>25</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>65</td>
<td>100</td>
<td>7.37</td>
<td></td>
</tr>
</tbody>
</table>

Fig.8 Stacking Analysis with power consumption [20]
As the technology is scaled day-by-day, the leakage is becoming a prime concern in the area of integrated circuit design. Low power memory is in great demand today for various applications and so we try to review the SRAM with low leakage current. As the technology is scaling day by day so the leakage reduction method is according to the new predictive technology. In this work, we compare the various SRAM circuits to get low leakage current at the new and different levels of device scaling. They are the conventional SRAM1, SRAM2 with power gating on the Vss line, the SRAM3 with power gating on the VDD line, and the SRAM4 with both on the VDD and Vss lines, respectively. Among the four SRAM, the SRAM2 shows the smallest amount of leakage, i.e., 2.73nA, because its sub-threshold leakage is most suppressed by its BODY and DIBL effects. Also, the study of the change in the threshold voltage or the thickness of gate-oxide of some transistor cells is done to decrease the leakage current without degrading its performance. By using five different configurations SRAM1,SRAM2,SRAM3,SRAM4 for the SRAM cells, we have achieved a low-leakage SRAM without sacrificing performance and area is achieved.

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