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Experimental Analysis of Parameter Limitations in High-Frequency Resonant Gate Driver

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***Abstract*—In megahertz switching frequency, the effect of loss is significant. In diode-clamped resonant gate driver circuit, the resonant inductor current, duty ratio and dead time are the limiting parameters which bring implications to the switching loss and hence total gate drive loss. The experimental analysis has been carried out to validate the simulation results. From the predetermined inductor current of 9 nH, duty ratio of 20 % and dead time of 15 ns, remarkably, the experimental results show less than 10 % difference in value compared to the simulation. Therefore, this new finding validates that by using correct choice of these values, the diode-clamped resonant gate driver can operate better in higher switching frequency.**

***Index Terms*—High Frequency, Limiting Parameters, Resonant Gate Drive, Switching Loss.**

I. Introduction

There have been many resonant gate drive (RGD) introduced in recent years and most of them looked for solution in switching loss reduction and improved efficiency with higher power output density. At high frequency operation, specifically above 1 MHz, the effect of gate drive circuit on overall performance becomes critical. Even though many circuit topologies employing LC resonant configuration techniques are applied [1-13], detailed analyses on switching loss and energy savings are yet to be further explored and verified.

A high frequency self-powered resonant gate driver has been introduced to improve power savings, reduce gate driving loss [1] and other studies concentrate on recovering the circulating energy in the circuit [4, 6, 9, 12]. More issues related to solving shoot-through current in the application of synchronous buck converter circuit are well described in [7]. In addition, to relate the importance of RGD, some reviews on high frequency converter design are presented in [14].

In the previous work, several gate driver topologies have been studied. Initially, the inductive coupled gate driver has been proposed where the power losses are investigated based on the turn-on cycle of gate voltage and inductor current [11]. Then a detailed study on the diode-clamped resonant gate driver is carried out in order to analyze the switching loss for specific limiting parameter values [13]. Subsequently, the extension of the work is presented in this paper to verify the simulation analyses of diode-clamped RGD circuit, Fig. 1 as discussed in the previous work [15] where energy recovery and power loss savings are observed.

The simulation work has shown that there are parameters which affect the design outcome of diode-clamped RGD circuit. Here, the design used must be based on optimized duty ratio, D, dead time, t_D and inductor value, L_r. These limiting parameters are important in achieving high frequency gate drive operation. From iterative numerical method, it is found that the D, t_D and L_r are 20 %, 15 ns and 9 nH respectively. This eventually gives results in lower total switching loss and yields better performance in high frequency environment.

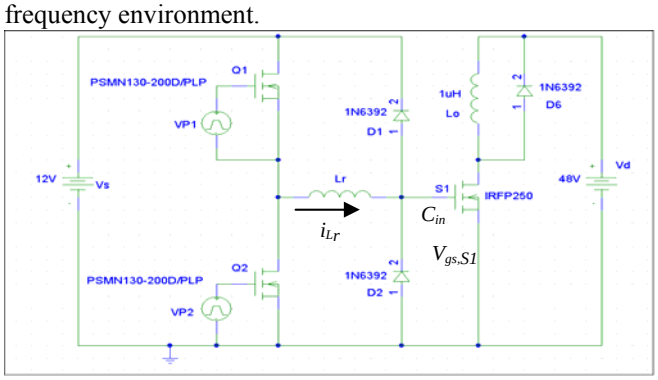

Fig.1 Diode-Clamped RGD Circuit [15]

The simulation was carried out according to circuit topology in Fig. 1 with high power MOSFETs are used. V_{P1} and V_{P2} are the two separate pulse width modulators (PWM) which provide complementary pulses to switch Q_1 and Q_2 respectively. The 5-V PWM input pulses are used to drive the switches with a t_D interval of 15 ns. The operating waveforms of the switches, the inductor current, i_{Lr} and the gate voltage of S_1, $V_{gs,S1}$ are shown in Fig. 2.

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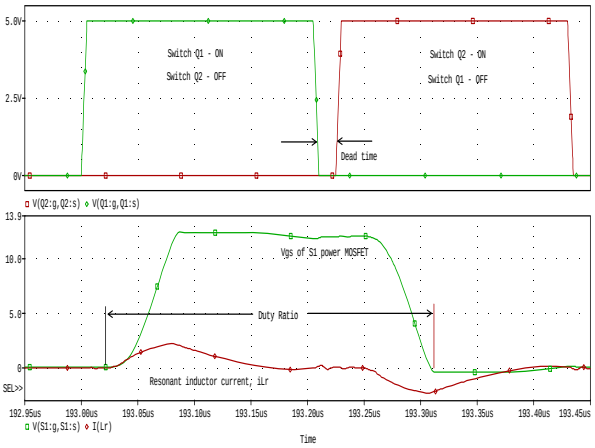

Fig. 2 Operating Waveforms of Diode-Clamped RGD Circuit [15]

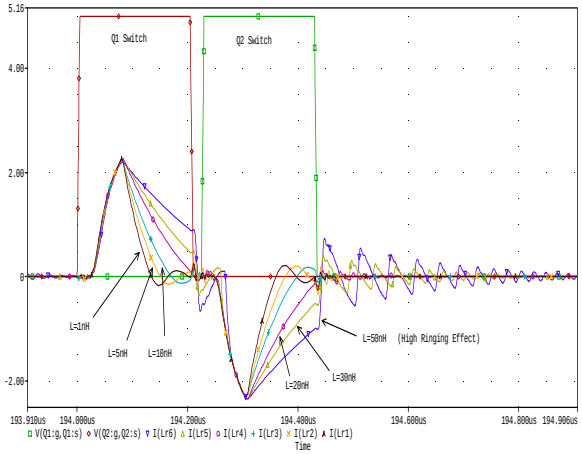

Fig. 3 Varying i_{Lr} for 20 % pulse width at t_D of 15 ns [15]

The circuit operation explains that as soon as Q_1 conducts, i_{Lr} starts to develop. Since Q_2 is OFF at this time, both i_{Lr} and $V_{gs,S1}$ are charged to maximum values. The duration of charging time depends on L_r and the resonant impedance of the network. Once they are fully charged, i_{Lr} will then discharge to zero through body diode of Q_2, L_r, D_1 and back to V_s. This current path indicates energy recovery saving mode where input current goes back to source at the end of the switching cycle. Then after t_D, Q_2 takes turn to conduct with Q_1 is now turned off. Here, i_{Lr} is once again charged but in the opposite direction. The $V_{gs,S1}$ approaches zero to a point where i_{Lr} is maximum. Similarly, the i_{Lr} is also discharged to zero from negative peak value through D_2, L_r, body diode of Q_1 and back to V_s. This circuit's symmetrical operation continues in the next subsequent switching cycles. However, the effectiveness of the RGD circuit depends on the values of the limiting parameters.

II. Limiting Parameters of Diode-Clamped RGD Circuit

The discussion on the limitations of the diode-clamped RGD circuit is very limited. The choice and values of components used, especially in L_r is important. The objective is to produce a small scale board with smaller size components. The summation of charging and discharging time of i_{Lr} is used as a benchmark in determining the minimum range of duty ratio, D. From Fig. 3, for fixed pulse width in V_{P1} and V_{P2}, an increase of L_r leads to higher oscillation counts at the end of its turn-off. Consequently, higher stress and dissipation will be experienced by the diode-clamped RGD circuit. On the other hand, reducing L_r will result in slower relative switching speed.

In numerical analysis, the i_{Lr} equation is given in (1) where R_g is the total gate resistance of around 1.5 Ω. The time taken for i_{Lr} to reach peak value is given in (2) which measure the maximum current value. The rise and recovery times of i_{Lr} are given in (3) and (4) respectively. These equations indicate the transition speed of the switching cycle. The faster iLr takes to reach peak value, the better the transition speed will be. This also applies to the recovery time.

$$i_{L_r}(t) = \frac{2V_s}{\sqrt{\frac{4L_r}{C_{in}} - R_g^{\,2}}} e^{-\frac{R_g}{2L_r}t} \sin\left(\frac{\sqrt{\frac{4L_r}{C_{in}} - R_g^{\,2}}}{2L_r}t\right) \quad (1)$$

$$t_{peak} = \frac{\tan^{-1}\left(\frac{2L_r\sqrt{\frac{4L_r}{C_{in}} - R_g^{\,2}}}{R_g}\right)}{2\sqrt{\frac{4L_r}{C_{in}} - R_g^{\,2}}} \quad (2)$$

$$t_{rise} = \frac{\pi}{2}\sqrt{L_r C_{in}} \quad (3)$$

$$t_{rec} = \pi\sqrt{L_r C_{in}} \quad (4)$$

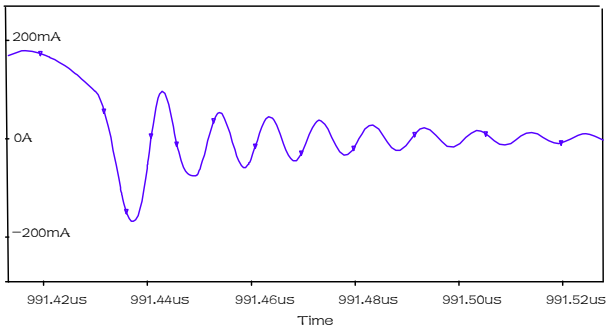

Fig. 4 Ringing during turn-off of i_{Lr} at t_D = 15 ns for L_r = 9 nH

Signal oscillation cannot be avoided especially in high frequency circuit. Fig. 4 shows that there is a presence of ringing in i_{Lr} which causes significant shift in power loss during $V_{gs,S1}$ turn-off. This is due to high parasitic inductance in the gate driver. However, the ringing margin is still low and can be accepted in the design.

In other aspect, t_D value can be obtained from the tradeoff between speed and power dissipation at turn-off. When t_D is set small, there exists more ringing counts. On the other hand, if t_D is applied too long, $V_{gs,S1}$ will appear floating leading to high power dissipation. In addition, the t_D value can be determined from the tradeoff between speed and high power dissipation also at $V_{gs,S1}$ turn-off. A longer t_D introduces higher ringing overshoot voltage. This pattern comes from the energy stored in the parasitic inductance when it is released across parasitic capacitance of S_1. Therefore based on the tradeoffs, t_D is optimized at 15 nH, as shown in Fig. 5 [15].

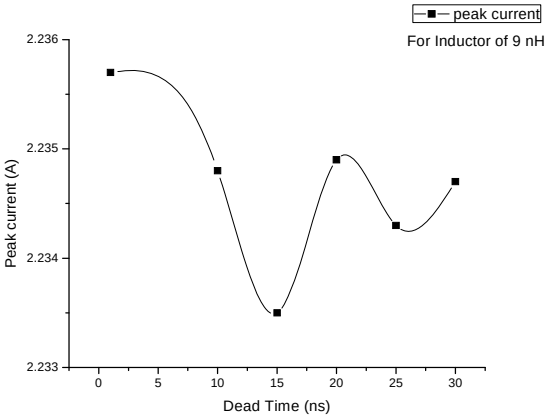

Fig. 5 Optimized t_D value at lowest peak current of i_{Lr}

III. Methodology

The experimentation took place in power electronics research lab with some of the components changed compared to simulation, due to the unavailability in local market. Since this is the preliminary experimental work, the difference in I/V ratings of the components used do not alter the results much compared to the simulation. The changes are shown in Table I and Table II.

TABLE I Components Used in Simulation

Simulation	
Component Name	Ratings
PSMN130-200D/PLP	200 V / 20 A, $R_{DS(ON)}$=0.130 Ω
1N6392	45 V / 60 A
IRFP250	200 V / 33 A, $R_{DS(ON)}$=0.085 Ω
V_D	48 V

TABLE II Components Used in Experiment

Experimentation	
Component Name	Ratings
STP22NF03L	30 V / 22 A, $R_{DS(ON)}$=0.038 Ω
SDP06S60	600 V / 6 A
IRFI540NPBF	100 V / 20 A, $R_{DS(ON)}$=0.052 Ω
V_D	25 V

The PWM signals are generated by dual-output arbitrary function generator (Tektronik AFG 3102). The gate driver is applied to the inductive chopper load. Here, the primary objective of the discrete experimental test-bed is to examine the effectiveness of gate driver circuit in megahertz switching frequency over a fixed load condition. A 12-V input voltage is used for gate drive circuit. The output switch, S_1 has successfully turned on and the experimental setups have shown correct operating waveforms similar to simulated waveforms as illustrated in Fig. 2. In addition, the PWM outputs from the function generators are fed into MOS driver (EL7104) before connecting to the gate of MOSFET switches, Q_1 and Q_2.

IV. Experimental Results

Two complementary PWM signals are applied to the drivers. The PIC or DSP chips can be used to generate these signals. However, for simplicity in duty ratio and dead time variation, the arbitrary function generator is chosen. For 1 MHz switching frequency there will be some noise appeared in the signals. Using MOS gate drivers and filter circuit, this noise can be reduced significantly. With 15 ns t_D applied in between Q_1 and Q_2, the output PWM signals of 20 % duty-ratio resulting from the MOS drivers are shown in Fig. 6.

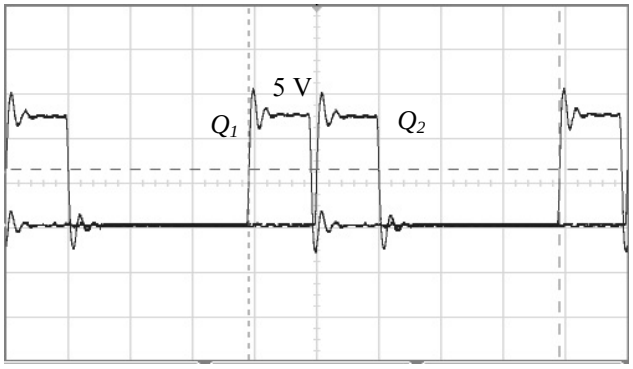

Fig. 6 PWM signals (y:2V/div, x:200ns/div)

These PWM signals are fed into two gate terminals of n-channel MOSFETs via driver chips. The experimental behavior of charging and discharging i_{Lr} is shown in Fig. 7. The positive peak current is about 3.2 A and the rise and recovery times taken by this current are about 25 ns and 50 ns respectively. This results show resemblance of i_{Lr} behavior found in the simulation.

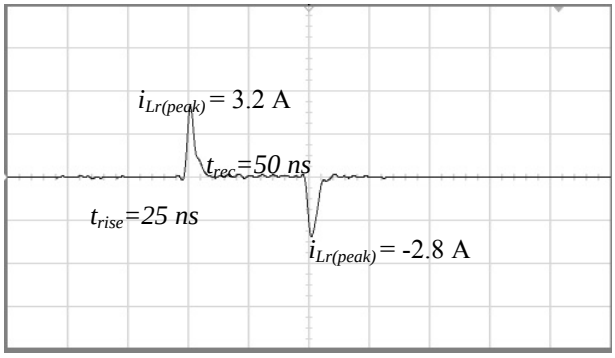

Fig. 7 Inductor current, i_{Lr} (y:2A/div, x:100ns/div)

The charging of i_{Lr} yields the charging of $V_{gs,S1}$ to maximum peak value of 5 V as shown in Fig. 8. This result matches the simulation result shown in Fig. 2. However, due to stray inductance experienced by the switch, caused by the load inductor, some noise is seen.

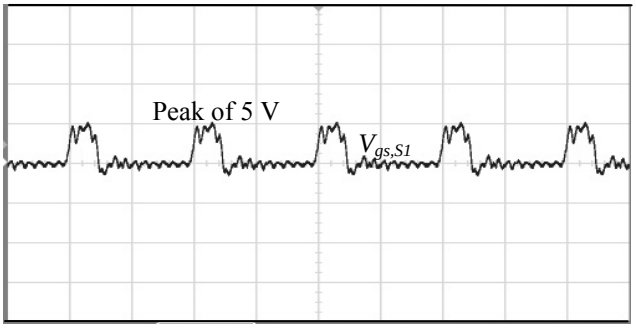

Fig. 8 $V_{gs,S1}$ output voltage (y:5V/div, x:500ns/div)

The noise also leads to the oscillation of i_{Lr} during turn-off. From simulation in Fig. 4, the ringing amplitude of 200 mA is observed. The experimental result shown in Fig. 9 proves this where the i_{Lr} is tapped and measured between -200 mA and 200 mA.

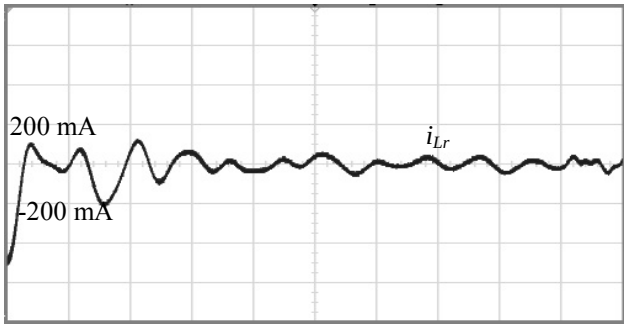

Fig. 9 i_{Lr} oscillation during turn-off (y:200mA/div, x:50ns/div)

In order to justify that switch S_1 conducts correctly, the drain current and voltage are also measured. Both of them correspond to the inductive load circuit where peak current and voltage measure 2 A and 22 V respectively which are true based on given load parameters.

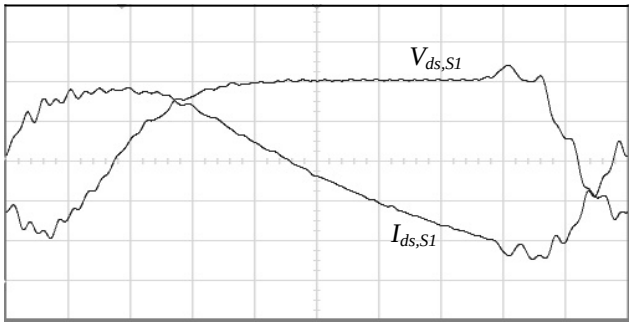

Fig. 10 I_{ds} (y:0.5A/div) and V_{ds} (y:5V/div) of S_1 (x:100ns/div)

Therefore, all of the experimental results validate the simulation work except some of the parameters and components used are not of the same types with the simulation. Nevertheless, the outcomes still show a definite proof of the work. The analysis of data is represented in the next section.

V. Results and Discussions

All three sets of data are analyzed based on different results taken from experiment, simulation and MathCad. The peak i_{Lr}, t_{rise}, t_{rec}, switching loss in Q_1, $P_{SW,Q1}$ and $P_{SW,Q2}$ are compared to validate the simulation results. The comparison is tabulated in Table III.

TABLE III Comparison of Data

	Experiment	Simulation	MathCad
$i_{Lr(peak)}$ A	3.2	2.4	3.6
t_{rise} (ns)	25	30	25.81
t_{rec} (ns)	50	58	51.62
$P_{SW,Q1}$ (mW)	425.2	418.02	420.34
$P_{SW,Q2}$ (mW)	438.5	453.47	447.80

The simulation data is taken from previous work [15]. The numerical analysis using MathCad is carried out to verify the results using the formula given in Eqn. (1) to Eqn. (4). From Table III, the experimental data validates the simulation work. In addition, MathCad calculation has shown and proven that the analysis is correct only with the difference of less than 10 %. However, the simulated peak i_{Lr} value indicates a significant different in result compared to others. This is caused by higher internal gate resistance in the driver used in the simulation setup. Other than that, the results show promising indicator for the RGD circuit to operate in high switching frequency with lower stress and better performance.

VI. Conclusion

This paper validates the simulation results obtained from PSpice simulation which was discussed in details in [15]. In diode-clamped resonant gate driver circuit, the predetermined parameter values such as inductor current, duty ratio and dead time have been justified via experimental analysis. When comparing the simulation results with experiment and MathCad calculation, the results show that the difference of less than 10 %. Therefore, this gate driver can be used in higher switching frequency with the specified parameter values.

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