Design of Optimized Reversible BCD Adder/Subtractor

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***Abstract*—Reversible logic has emerged as one of the most important research area in the past few decades. Reversible or information lossless circuits have applications in nanotechnology, digital signal processing, communication, computer graphics and cryptography. It is also a fundamental requirement in the emerging field of quantum computing. In this paper an optimized method is proposed to realize a reversible Binary Coded Decimal (BCD) adder/subtractor circuit. In order to optimize the design, nines compliment gate (NCG) and BSCL gates are proposed. This proposed reversible BCD adder/subtractor is evaluated and optimized in terms of gate count, constant inputs and garbage outputs.**

***Index Terms*—Basic reversible gates; Reversible BCD adder; Reversible BCD subtractor; Constant input; Garbage; Gate count; Optimization.**

I. Introduction

Classical computing devices process large amount of digital data using logical (Boolean) operations. A single bit of information is erased after every logical operation. Landauer proposed that KT ln(2) joules of energy are lost for erasing a single bit of data, where K is the Boltzmann's constant and T is the absolute temperature at which computation is performed [18].

Energy dissipation is one of the major issues in present day technology. Improvement in technology leads to compactness in size of system and increase in execution speed. Due to this energy dissipation is increased by the system. The logical circuits used in these systems are called irreversible systems.

Charles Bennet proposed a theoretical background which proved that reversible general purpose computing devices can be built [1, 2]. This gave rise to reversible logic circuits. Logical reversibility means that after finishing a computation, it is possible to retrace every step and reconstruct data which was used in every step. Thus, reversible logic circuits offer an alternative that allows computation with very small energy dissipation.

The main objective of this paper is to perform both BCD addition and BCD subtraction in a single circuit with minimum number of garbage gate count and constant input. To achieve the operation of reversible BCD addition and subtraction in a single circuit two new gates are proposed which are optimized such that it doesn't possess any restrictions of reversible gates as mentioned above. It has been proved that the proposed reversible BCD arithmetic circuit is better than the existing logics in the literature; in terms of number of garbage outputs, constants inputs and the gate count.

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II. Background of Basic Reversible Gates

Consider following issues to perform synthesis of reversible gates

- The number of outputs of a reversible logic gate should be equal to the number of inputs.
- The output of the gate that is not used as a primary output or as input to other gate is called garbage outputs. A heavy price is paid for every garbage outputs.
- The number of constant input to the gate should be as minimum as possible.
- In reversible logic, fan-out of more than one is not allowed; every output can be used only once [19].

III. Conventional BCD Adder and Subtractor

A Binary Coded Decimal (BCD) adder is a circuit which adds two 4-bit BCD numbers in parallel and produces a 4-bit BCD result. Fig. 1 shows the block diagram of conventional BCD adder. The circuit must include the correction logic to produce valid BCD output. Two 4-bit BCD numbers X and Y along with carry input is added using conventional 4-bit parallel adder, 4-bit sum and a carry is taken out. If the carry output is set or if the result is greater than nine, binary 0110 is added to the intermediate sum output with the help of second stage 4-bit parallel adder circuit.

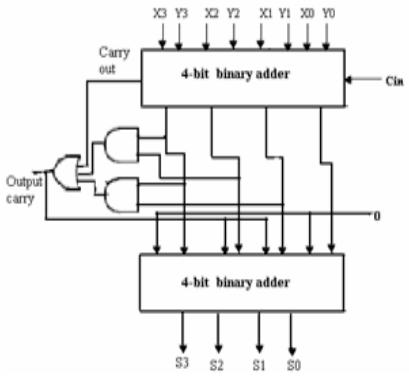

Fig. 1 Block diagram of conventional 4-bit BCD adder

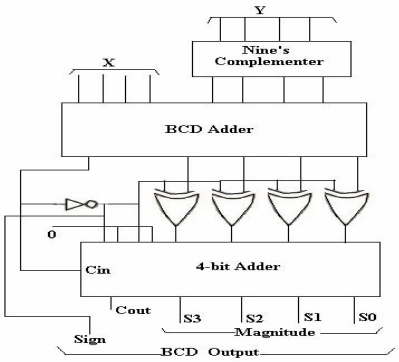

Fig. 2 BCD Subtractor

To perform BCD subtraction BCD number X and nines compliment of Y is added by using conventional BCD adder. If carry output is 0 then nines compliment of BCD adder

ouput is taken out or if carry out put is 1 then 0001 is added to the BCD adder output to get the corrected valid magnitude subtraction output.In each case carry out of the BCD adder is complimented and taken as Barrow output.The conventional block diagram of BCD subtractor is shown in fig 2.

IV. Survey of Reversible BCD Adder Circuits

In the literature there exist several reversible BCD adder and BCD subtractor. Here few of those are chosen based on constant inputs, garbage outputs and the gate count. Fig. 3 depicts the block diagram of one of the 4-bit reversible BCD adder considered [6].The 4-bit reversible parallel adder internally has four1-bit full adder gates. Here each 1-bit full adder is implemented using New Gate, NG [14] and New Toffoli Gate, NTG [7] gates with single constant input and two garbage outputs. The implementation of the first4-bit reversible adder requires five constant inputs and produces eight garbage outputs.

In this case the correction logic is implemented using a combinational logic and four Feynman, FG [15] gates. Each Feynman gate requires one constant input. The combinational logic is implemented using three NG gates, which requires three constant inputs and gives out six garbage outputs. Four FG gates are used to pass the input to overcome fan-out limitations. The second 4-bit reversible parallel adder circuit requires two more constant inputs and thus it uses 6 constant inputs and produces eight garbage outputs. This circuit totally requires 23 gates, 22 garbage outputs and 17 constant inputs.

Fig. 4 shows the block diagram of another BCD adder [12, 13]. Here the 4-bit reversible parallel adder is implemented using HNG gate; this uses four gates, four constant inputs and produces eight garbage outputs. For two 4-bit parallel adder circuits it requires 8 gates 16 garbage outputs and 8 constant inputs. The second 4-bit reversible binary parallel adder uses two more extra constant inputs. The Correction logic requires six gates, seven constant inputs and the gate produces six garbage outputs. To overcome the fan-out limitations, FG and HNFG gates are used that is to obtain more than one copy of the input. The overall implementation of BCD adder using this logic[13] requires 14 gates, 17 constant inputs and produces 22 garbage outputs.

Fig. 5 depicts the implementation of BCD adder using TSG gate [20].This adder is constructed without considering fan-out limitation. As in previous case, this adder also uses two reversible parallel adders which require eight gates and nine constant inputs, producing 16 garbage outputs. The correction logic is constructed using three NG gates with three constant inputs while producing six garbage outputs. To construct complete reversible BCD adder circuit, 11 gates and 11constant inputs are required, producing 22 garbage outputs.

The implementation of BCD adder given in Fig. 6 uses two Fredkin gates, FRG and one Toffoli Gate, TG [22] for the overflow detection logic, with one constant input and one garbage output [9]. The Correction logic also uses three gates FG, TSG and Peres gate, PG [15], with two constant inputs and two garbage outputs. It uses a 4-bit parallel adder constructed using four TSG gates, with four constant inputs and eight garbage outputs. Collectively this implementation requires ten gates, seven constant inputs and produces 11 garbage outputs.

The reversible BCD adder depicted in Fig. 7 uses a single SCL gate to perform correction logic [5]. In this implementation, the 4-bit parallel adder is constructed by using 4 HNFG gate with four constant inputs and eight garbage outputs. In order to generate corrected BCD sum PG, HNG, and FG gates are used with two input constants and two garbage outputs. This BCD adder implementation has ten garbage outputs, gate count of eight and six constant inputs.

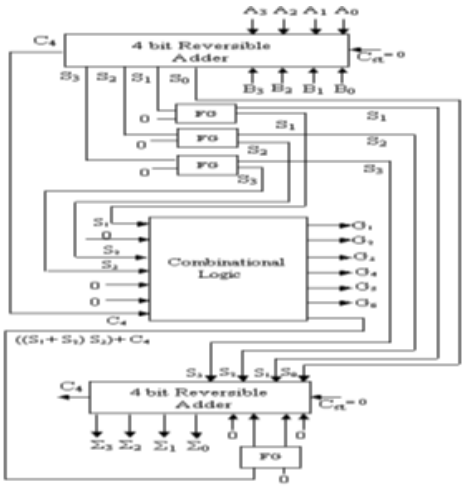

Fig. 3 Block diagram of reversible BCD adder [6]

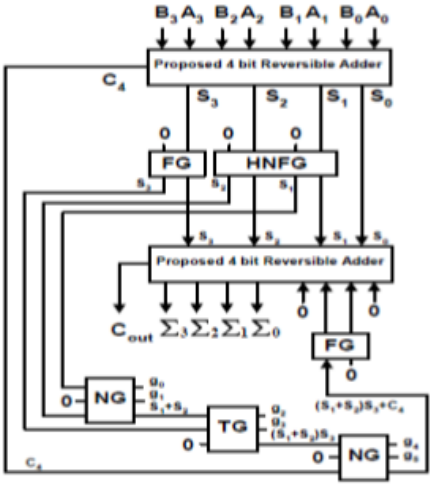

Fig. 4 Block diagram of reversible BCD adder [12]

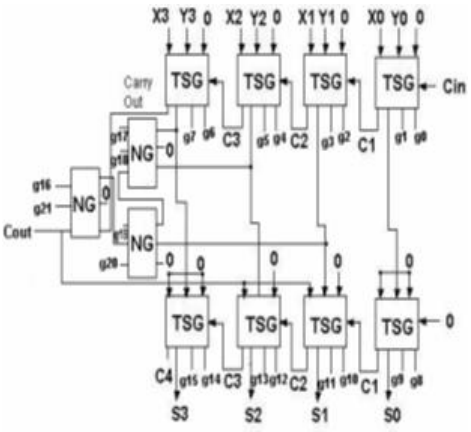

Fig. 5 Block diagram of reversible BCD adder [19]

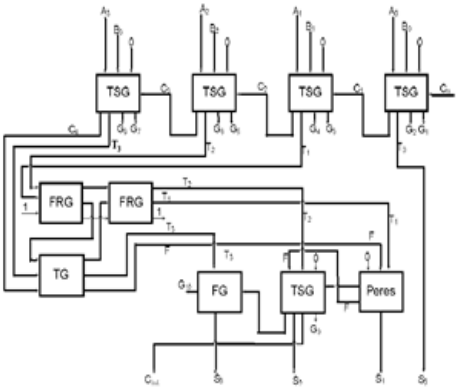

Fig. 6 Block diagram of reversible BCD adder [8]

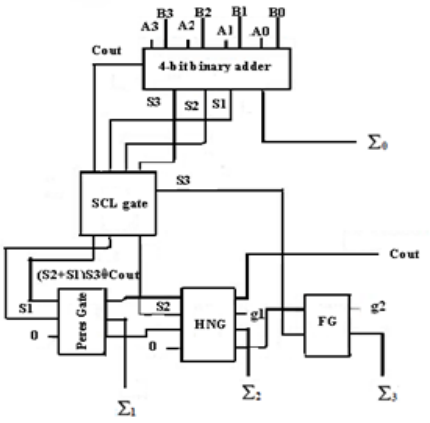

Fig. 7 Block diagram of reversible BCD adder [5]

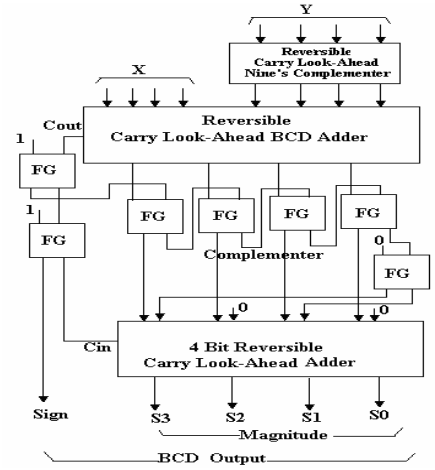

Fig. 8 Reversible Carry Look-Ahead BCD Subtractor

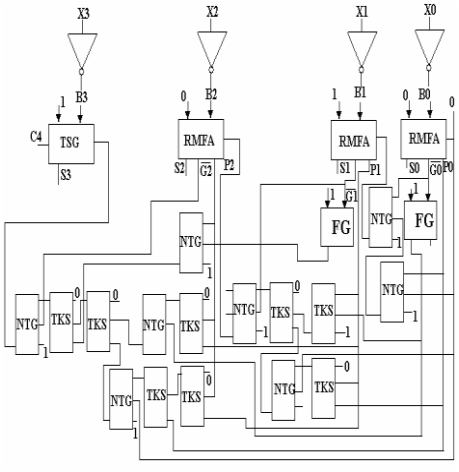

Fig. 9 Reversible Nine's Complementer

The existing reversible BCD subtractor [8] is as shown in fig 8. To design BCD subtractor nines compliment circuit is required which is shown in fig 9.Here to design nines compliment circuit gate count required is very high which is 26 . To design the entire circuit existing BCD subtractor requires 106 gates, garbage outputs as 154 and 87 constant inputs. Therefore hardware required to construct BCD subtractor is very high and it produces a very high number of garbage's.

V. Proposed BCD Adder/ Subtractor

In order to design a basic 4- bit reversible BCD adder/subtractor two new reversible gates are proposed.

- NCG(5*5)
- BSCL(6*6)

A. NCG[Nines compliment gate]

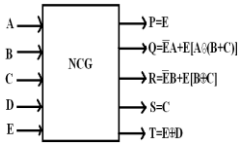

Fig. 10 Nines compliment gate[NCG]

In this paper, a new 5X5 reversible Nines compliment gate [NCG] is proposed. The objective of this gate is to obtain the pass/nines compliment of the given number depending on the control signal E. The NCG takes the inputs A, B, C, D and E and produces the outputs P, Q, R, S and T. Corresponding output functionalities are shown in Fig 10. The key feature of this NCG is when control signal E is equal to zero, four bit binary number is directly passed to the output Q, R, S and T .When E is equal to one then, Q, R, S and T is equal to nines compliment of the number A, B ,C and D. Therefore depending on control signal E, either pass/nine's compliment outputs will be available on output Q, R, S and T.

B. BCD adder constructed using CL gate

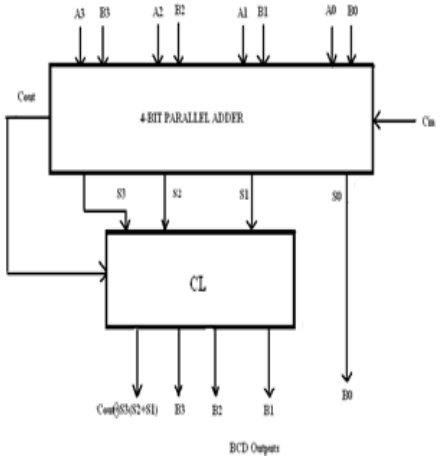

Fig. 11 BCD adder using CLgate

The implementation of existing 4-bit reversible BCD adder [21] is depicted in Fig. 11. In this reversible BCD adder, 4-bit reversible parallel adder is implemented by using the reversible PTR gate [16]. The PTR gate is chosen to perform this operation because its length of the critical path in turn it increase the speed of operation. The PTR gate performing as a single reversible full adder is depicted in the Fig. 12.The block diagram of four bit parallel adder

constructed by using PTR gate is depicted in fig.13. The gate count and constant inputs needed to construct a 4-bit parallel adder are four and garbage output of eight.

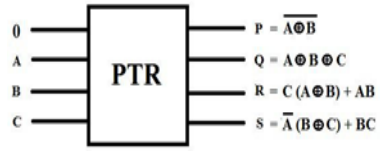

Fig. 12 PTR gate as a single full adder

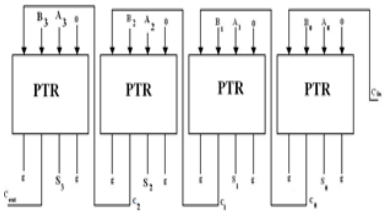

Fig. 13 4-bit reversible parallel adder using PTR gate

If the carry is generated from the reversible 4-bit parallel adder or its sum is greater than nine, then decimal number 6 is added to the sum to produce valid BCD output. In literature it is found that to perform this operation separate logic circuitry such as detection of overflow, correction logic decider and final addition of decimal number are used. This results in use of more number of reversible gates, constant inputs and producing a large number of garbage outputs. In the proposed reversible BCD adder logic, overflow detection logic operation, correction logic operation and final addition operations are performed by a single 4x4 CL gate. The CL gate takes the input C_{out}, S_3, S_2 and S_1 which are the outputs of 4-bit reversible parallel adder and generates valid BCD sum outputs B_3, B_2, B_1 and B_0 and a Carry output. Since the CL gate requires no constant inputs and generates no garbage outputs, the number of constant inputs and garbage outputs to build the proposed logic completely is same as that of the constant inputs and garbage outputs generated from the reversible parallel adder.

C. BSCL gate

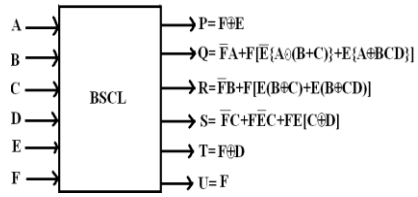

Fig. 14 BSCL gate

Here a new 6X6 BCD subtraction correction logic [BSCL] gate has been proposed.Block diagram and its corresponding functionalities is depicted in fig 14. The purpose of this gate is either to find correction logic for BCD subtraction or to pass same data to the output depending on the control signal.Here F is the control signal ,if F is equal to 0 E A B C and D as it is passed to the output P Q R S and T. If F is equal to 1, then output Q R S and T depends on the value of E. If E is equal to 0 then Q R S and T is the nines compliment of the input binary number A B C and D. If E is equal to 1 then binary number 0001 is added to ABCD to get the valid corrected subtraction result.

D. Block diagram of proposed BCD adder/subtractor

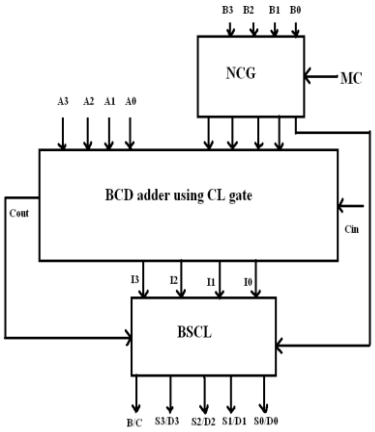

Fig. 15 BCD adder /subtractor

The block diagram of 4-bit BCD adder/subtractor using proposed NCG and BSCL gate is as shown in fig 15. The designed block acts as a BCD adder/ subtractor depending on the control signal MC [master control]. Four bit BCD numbers A(A3 A2 A1 A0) and B (B3 B2 B1 B0) are given as input to the block.Depending on the control signal MC either BCD number A and B are added or subtracted.If MC is equal to 0 then BCD addition is performed and if MC is equal to1 BCD subtraction is performed. Here if MC is 0 B3 B2 B1 and B0 are as it is passed to the output and BCD number A (A3 A2 A1 A0) and B (B3 B2 B1 B0) are added along with the input carry using BCD adder constructed by using CL gate. And the result of BCD adder is designated as intermediate result I3 I2 I1 and I0.Since MC is equal to 0 intermediate results and carry out of the BCD adder is directly passed by BSCL gate to sum (S3 S2 S1 S0) and carry (C) output of the block. If MC is equal to 1the output of NCG is nine's compliment of input B3 B2 B1 and B0.Therefore BCD number A (A3 A2 A1 A0) and nine's compliment of B (B3 B2 B1 B0) are added by using BCD adder using CL gate to obtain intermediate results of the BCD subtraction I3 I2 I1 and I0.Since MC is equal to 1 subtraction correction is done by using BSCL gate. This subtraction correction is dependent on the carry out of the BCD adder.If Cout of the BCD adder is 0 then difference of A and B that is D3 D2 D1 and D0 is obtained by taking nines compliment of the intermediate result I3 I2 I1 and I0 and Barrow B is equal to the compliment of cout of the BCD adder. If Cout of the BCD adder is 1 then D3 D2 D1 and D0 is obtained by adding 0001 to the intermediate result to get valid corrected subtraction result.This entire subtraction correction is efficiently done by BSCL gate. Since both NCG and BSCL are controlled by the same (constant) control signal, one constant input can be reduced by taking the ouput of NCG which is same as passed value of MC. Thus it reduces one garbage output of NCG and also the constant input required for BSCL gate. Hence this optimized BCD adder / subtractor block requires gate count as 7, garbage output as 9 and 5 constant inputs.

VI. RESULTS

Comparative study of different reversible BCD adder logic is depicted in Table. I. It gives the comparison of the different designs in terms of the optimization parameters. This table clearly indicates that proposed BCD

adder/subtractor is highly optimized in terms of gate count garbage outputs and constant inputs.

TABLE. 1 COMPARISION TABLE

	Gate count	Garbages	constant in put	function
[6]	23	22	17	BCD adder
[13]	14	22	17	BCD adder
[20]	11	22	11	BCD adder
[9]	10	11	7	BCD adder
[5]	8	10	6	BCD adder
[8]	106	154	87	BCD subtractor
proposed	7	9	5	BCD adder/subtractor

VII. CONCLUSION

The proposed reversible BCD adder can be used for designing large reversible systems, which is can be used in ultra low power digital circuits and quantum computers. Analyses of various implementations discussed are tabulated in Table. I. It is observed that the proposed logic is optimized compared to other design methods. Due to optimization the power dissipation, speed and hardware complexity is reduced.

REFERENCES

[1] C.H.Bennett, 1973. Logical reversibility of computation, IBMJ. Research and Development,17: 525 - 532.

[2] C.H.Bennett."The thermodynamics of computation – A Review", *International journal of Theoretical Physics*, 21:905-928,1982.

[3] Dan C.Marinescu and Gabriela M.Marinescu, "Approaching Quantum Computing", 2005 pp. 1-41.

[4] E. Fredkin, T Toffoli, "Conservative Logic", International Journal of Theor. Physics, 21(1982), pp.219-253.

[5] H R Bhagyalakshmi,M K Venkatesh "Optimized reversible BCD adder using new reversible logic gates"journal of computing VOLUME 2, ISSUE 2, FEBRUARY 2010, ISSN 2151-9617.

[6] Hafiz Md. Hasan Babu and A. R. Chowdhury, Design of a Reversible Binary Coded Decimal Adder by Using Reversible 4-bit Parallel adder , VLSI Design 2005, pp.255-260, Kolkata, India,Jan 2005.

[7] Hafiz Md.Hasan Babu, Md. Rafiqul Islam, Ahsan Raja Chowdhury and Syed Mostahed Ali Chowdhury, "On the realization of reversiblefull-adder circuit", *International Conference on Computer and Information Technology, Dhaka, Bangladesh,* 2003, pp. 880-883.

[8] Himanshu Thapliyal and Sumedha K. Gupta "Design of Novel Reversible Carry Look-Ahead BCD Subtractor" *9th International Conference on Information Technology (ICIT'06) 2006 IEEE*

[9] K.Biswas,et.al., "Efficient approaches for designingreversible Binary Coded Decimal adders'' *Microelectron, J(2008)doi:10.10.16/j.mejo.2008.04.003.*

[10] L.M.K Vandersypen, M. Steffen, G.Breyta, C.S. Yannoni, M.H. Sherwood and I.S Chuang. "Experimental realization of Shor's Quantam Factoring Algorithm Using Nuclear Magnetic Resonance", *Nature,2001 414*: pp. 883-887

[11] M. A. Nielsen and I. L. Chuang, Quantum Computation and Quantum Information. Cambridge, U.K.: Cambridge Univ. Press, Dec.2000.

[12] M. Haghparast and K. Navi, 2007. A Novel Reversible FullAdder Circuit for Nanotechnology Based Systems. J. AppliedSci., 7 (24): 3995-4000.

[13] M. Haghparast and K. Navi, 2008. A Novel reversible BCDadder for nanotechnology based systems. Am. J. Applied Sci., 5(3): 282-288.

[14] Md. M. H Azad Khan, "Design of Full-adder With Reversible Gates, *International Conference on Computerand Information Technology*, Dhaka, Bangladesh, 2002,pp.515 to 519.

[15] Peres, A.1985. Reversible logic and quantum computers, Physical Review: A, 32 (6): 3266-3276.

[16] Praveen B, Tilak B.G, Rashmi S.B. "A Novel High Speed Reversible Adder/Subtractor", *Proceedings of the 3rdInternational Conference on Computer Modelling and Simulations, ICCMS, jan 7-9, 2011.*

[17] R. Feynman, "Quantum Mechanical Computers", *Optic News,* Vol. 11, pp. 11-20, 1985.

[18] R.Landauer, 1961. Irreversibility and heat generation in thecomputing process,IBM J.Research and Development,5 (3):183-191.

[19] Robert Wille, Rolf Drechsler "Towards a Design Flow for Reversible Logic", (9-13).

[20] Thapliyal H., S. Kotiyal, M. B. Srinivas, 2006.Novel BCD adders and their reversible logic implementation for IEEE 754r format. Proceedings of the 19th International Conference on VLSI Design,3 7 Jan 2006 .

[21] Tilak B.G, Rashmi S.B and Praveen B"A Novel Optimized Reversible BCD Adder using reversible CL gate", *Proceedings of the 3rdInternational Conference on Computer Modelling and Simulations, ICCMS, jan 7-9, 2011.*

[22] Toffoli T, 1980. Reversible computing, Tech Memo MIT/LCS/TM-151. MIT Lab for Computer Science.